CSCE 613
Lab 5
Development and Simulation of Full Standard Cell Library
Due Date: 10/18/06

Introduction

In this lab you will design, simulate, characterize, and package a full standard cell library. While the tutorials demonstrated the design of a minimal cell library, your cell library will contain several additional cells in order to achieve more efficient logic synthesis.

Table 1 outlines a minimal set of cells for your library, but you may add additional cells if you wish (adding additional cells may make it easier for you to meet your design goals for the course project). You may design and layout each cell however you wish as long as each implements the specified digital logic function.

Name	Description
INVX1	inverter, NW=10λ, PW=20λ
INVX2	inverter, NW=20λ, PW=40λ
INVX4	inverter, NW=40λ, PW=80λ
INVX8	inverter, NW=80λ, PW=160λ
BUFX2	buffer (2 series inverters), NW=20λ, PW=40λ
BUFX4	buffer (2 series inverters), NW=40λ, PW=80λ
CLKBUF1	clock buffer (4 series tapered inverters) NW=[10, 20, 40, 40] λ, PW=[20, 40, 80, 80] λ
TINVX2	tristate inverter (**see Fig. 1.26 in textbook**) NW=20λ, PW=40λ
NAND2X1	2-input NAND gate, NW=10λ, PW=20λ
NAND3X1	3-input NAND gate, NW=10λ, PW=20λ
NAND4X1	4-input NAND gate, NW=10λ, PW=20λ
NOR2X1	2-input NOR gate, NW=10λ, PW=20λ
NOR3X1	3-input NOR gate, NW=10λ, PW=20λ
NOR4X1	4-input NOR gate, NW=10λ, PW=20λ
XOR2X1	2-input XOR gate, NW=10λ, PW=20λ
AOIX1	3-input AND-OR-INVERT, NW=10λ, PW=20λ
OAIX1	3-input OR-AND-INVERT, NW=10λ, PW=20λ
FAX1	1-bit full adder, NW=10λ, PW=20λ
HAX1	1-bit half adder, NW=10λ, PW=20λ
MUX2	2-input MUX, NW=10λ, PW=20λ
FILL	fill cell (layout only)
DFFX1	rising or falling-edge D-flip-flop (may or may not have built-in asynchronous reset), NW=10λ, PW=20λ

Table 1

Design Flow

Tutorials 1 (*schematic design*), 2 (*layout design*) and 3 (*preparing your cell library*) will assist you in developing your cell library. Tutorials 4 (*characterization*) and 5 (*abstract generation*) will assist you in performing the post-processing steps in order to prepare your library for use in the synthesis and place-and-route tools.

Requirements
For each cell, you must perform the following design steps:

1. Design cell schematic
2. Exhaustively test all possible input combinations using a test bench
3. Design cell layout
4. Extract layout
5. Perform LVS and analog extraction
6. Repeat testbench using analog_extracted view

Once you've completed design and testing, you must characterize your library using SignalStorm and generate abstracts with Abstract Generator.

Make sure you design each of your cells on a reasonable routing grid. You don't have to use the routing grid from the tutorials (4.5μ grid/2.25μ offset), but keep in mind that the minimum routing grid for metal1 and metal2 is 2.1 μm and the minimum routing grid for metal3 is 2.7 μm based on the minimum contact sizes and minimum metal spacing (for routing tracks).

What to Submit
Submit the cell schematic, layout, testbench simulation plot (from extracted layout), and HTML output of characterization data (from SignalStorm) for each of your cells.