# CSCE 613
# Lab 4
# Characterization of AMI C5N Devices Part 3
# Due Date: 10/4

**Task 1: Parasitic Capacitance**

Parasitic capacitance is the capacitance that is contributed by the source and drain. This includes gate-to-diffusion overlap and diffusion reverse-bias diode capacitance, as a function of diffusion area and perimeter (area is used for "vertical" diffusion diode capacitance; perimeter is used for the horizontal diffusion diode capacitance based on the thickness of the diffusion region). Like gate capacitance, this value is voltage-dependent. However, we can still estimate the average parasitic capacitance over the switching time.

Figure 2 shows a circuit that can be used to estimate these capacitances.

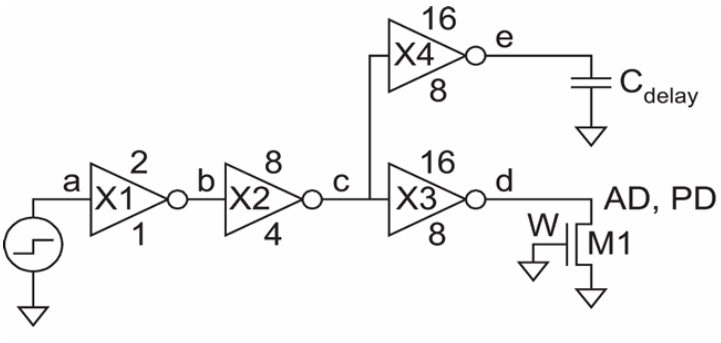


**Figure 2**

In this circuit, X3 drives the drain of an OFF transistor M1. This transistor's drain diffusion area (AD) and drain perimeter (PD) are computed automatically based on its channel width. X3 drives a capacitor whose value may be matched such that the delay of X3 and X4 are equal. This is the effective capacitance of M1's **drain**. Determine the capacitance per micron of width by normalizing the value of the width of M1.

**Repeat this test for the PMOS transistor. In this case, you'll need to reverse the direction of the PMOS and tie the gate voltage to $V_{dd}$.**