

CSCE 613
Lab 3
Characterization of AMI C5N Devices Part 2
Due Date: 10/4

Introduction

In this lab you will continue to characterize the AMI C5N PMOS and NMOS devices.

Task 1: Gate Capacitance

Gate capacitance is voltage-dependent, but we can still obtain an effective capacitance averaged across the switching time.

Figure 1 shows an FO4 circuit that may be used to determine gate capacitance. Setup this circuit like you did in Lab 1, but this time the goal is to adjust C_{delay} until the delay from c to g equals the delay from c to d. **This includes logic delay as well as switching time.** In this circuit, X3 and X6 have the same input slope and are of the same size, so when the total delay is matched, C_{delay} will have the same input capacitance as X4. Note that the **Xn** notation refers only to instance name and **NOT** the size of the transistor. Also note that rising and falling delay may not be equal, so measure the corresponding capacitance for both and determine the average.

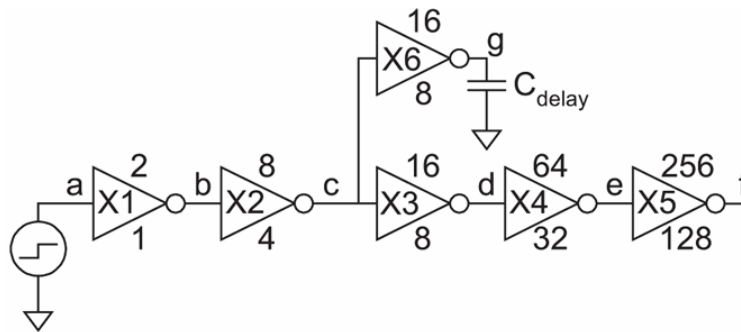


Figure 1

Once you determine C_{delay} , you must divide this value by the **total** gate width (in μm) contained within X4 to obtain the capacitance-per-micron of gate width ($C_{permicron}$). In order to set an initial (starting point) capacitance, refer to the gate capacitance estimation discussion in Chapter 2.

In order to isolate gate capacitance, you must set the source and drain area and perimeter to 0 for the FETs in X3 and X6 in order to remove the effects of parasitic (source/drain) capacitance.

Task 2: Effective Resistance

Now that we have determined the per- μ gate capacitance C_g and parasitic capacitance C_d for the NMOS and PMOS, we can now estimate the resistance of R_n and R_p (for NMOS and PMOS) using the switch-level delay model. To do this, you may calculate the differences in delay for inverters with different fanouts.

In Lab 1, you determined the rising and falling delay for a fanout-of-4 inverter. When you did this, you setup an inverter chain like the one shown in Figure 3.

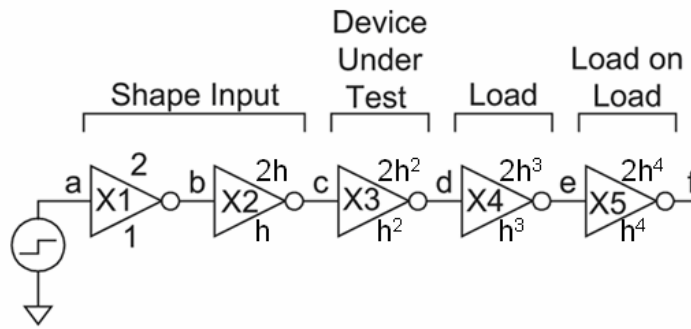


Figure 3

Figure 3 is more generalized than Figure 1 in Lab 1. Figure 3 shows a fanout-of- h inverter chain. In lab 1, $h=4$.

This yields the effective RC-model shown in Figure 4 (shown for X3 pulling down and pulling up).

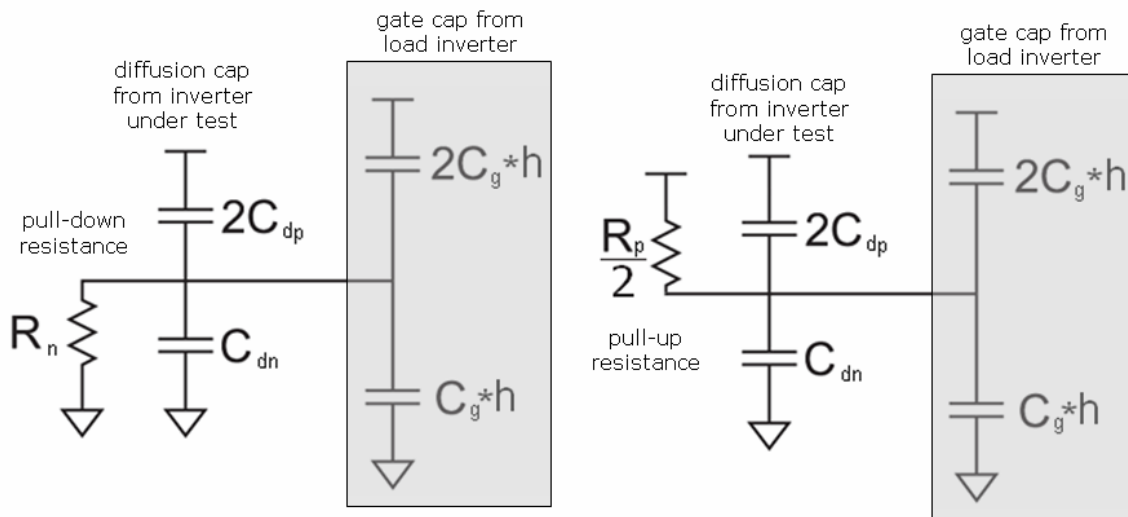


Figure 4

In this case, the delay may be calculated as $t = R_n * [(2C_{dp} + C_{dn}) + 3hC_g]$, where C_g is the NMOS gate capacitance and $C_{d(n|p)}$ is the diffusion capacitance (representing the drain terminals of the load inverter's PMOS NMOS). Note that the source capacitance doesn't affect the circuit, because the sources forms a parasitic capacitor where both plates are V_{dd} (for PMOS) or ground (for NMOS) and thus doesn't have any affect on the delay of the circuit.

Repeat your experiment from Lab 1, but this time measure the **rise and fall times** (switching time) for the inverter-under-test's output (as opposed to the rise and fall *delays*). Use the 90%/10% method to determine the beginning and end of a rising and falling edge.

Next, adjust the inverter sizes over the entire design (internal FET widths) such that $h=3$. Once you do this, measure the rise and fall times for the inverter-under-test.

Using the difference in these delays along with the gate and parasitic capacitance, you can use the following two equations to determine the effective resistance of both the NMOS and PMOS in the ON state.

$$\Delta t_r = \frac{R_p}{2} (3 \cdot h_h \cdot C_g + C_{dn} + 2C_{dp}) - \frac{R_n}{2} (3 \cdot h_l \cdot C_g + C_{dn} + 2C_{dp})$$

$$\Delta t_f = R_n (3 \cdot h_h \cdot C_g + C_{dn} + 2C_{dp}) - R_p (3 \cdot h_l \cdot C_g + C_{dn} + 2C_{dp})$$

In these equations, Δt_r and Δt_f represent the difference in rise and fall delay, respectively. h_h (=4) and h_l (=3) represent the value of h for the high-fanout and low-fanout, respectively. C_g refers to the gate capacitance, and C_{dn} and C_{dp} refers to the parasitic (drain) capacitance for the NMOS and PMOS, respectively.

Note that the drain capacitance cancels out in the equations above. Therefore, assuming $h_h = 4$ and $h_l = 3$, the equations can be re-written as:

$$\Delta t_r = \frac{3}{2} R_p C_g$$

$$\Delta t_f = 3 R_n C_g$$

Use these equations to solve for R_n and R_p .

What to Submit

As in lab 1, submit your designs and simulation results.