CSCE 613
Lab 2
Characterization of AMI C5N Devices Part 1
Due Date: 10/2

Introduction

As explained in Lab 1, SPICE (Spectre) MOSFET models have many parameters. However, these parameters can not be directly used to determine transistor performance information. This is why it is common for designers to run a series of device simulations when beginning to work with a new fabrication technology. In this lab, you will use several simulation techniques to determine behavioral characteristics for the NMOS and PMOS devices.

Task 1: I-V Characteristics: Fixed V_{gs}

In this task, you will characterize I-V characteristics assuming a fixed V_{gs}. You may use the schematics in Figures 1 and 2 to set up your tests. As shown, V_{ds} and V_{gs} are set using DC sources with a variable for their DC value. These variables must also be setup in Spectre. In Spectre, add the variables by selecting Variables | Edit and enter the variable name with appropriate values.

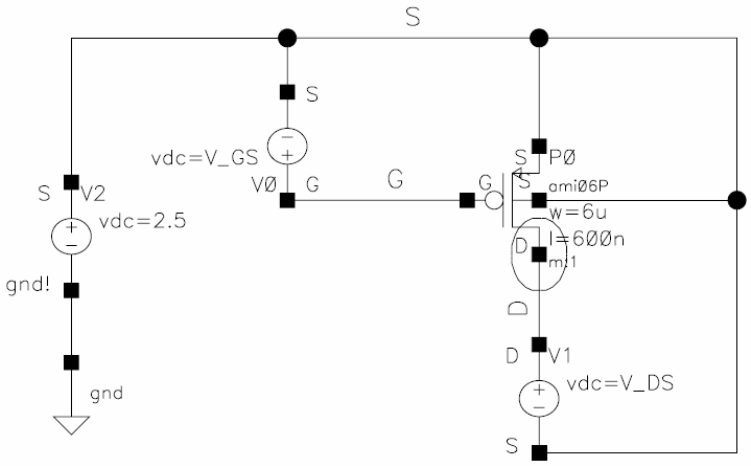

Figure 1: Schematic for PMOS test

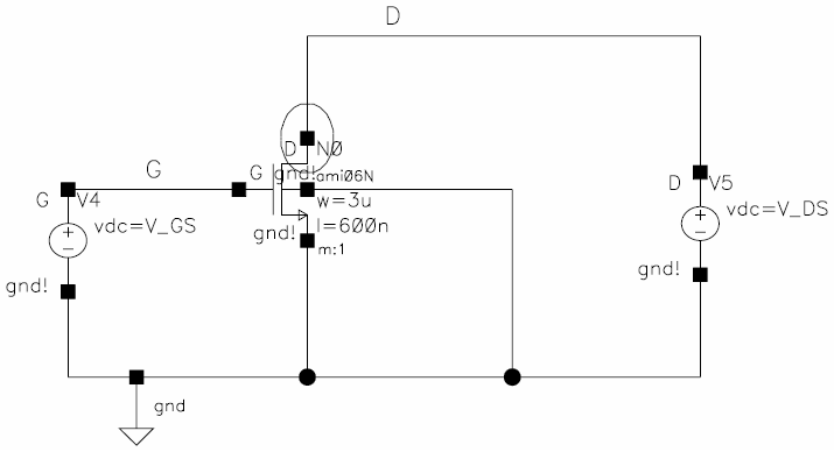

Figure 2: Schematic for NMOS test

For this task, set the variable value for V_{gs} as needed. The value of V_{ds} doesn't matter, since you'll tell the simulator to sweep this value (although you will have to set it).

Add a DC Analysis, select "Design Variable" as the Sweep Variable, specify the variable name, and finally a start and end value. Select the **drain** terminal on the transistor to plot as a ***current*** output.

Generate I_{ds}-V_{ds} curves for the PMOS and NMOS transistor by sweeping $\mathbf{V_{ds}}$ over the range [-2.5 0] and [0 2.5], respectively. Run simulations for fixed $\mathbf{V_{gs}}$ values of [-0.6 -0.9 -1.2 -1.5 -1.8] for the PMOS and [0.6 0.9 1.2 1.5 1.8] for the NMOS. This will ultimately yield five separate plots for each transistor.

Note: you can instantiate five transistors (and supporting wiring) in one schematic, each having independent $\mathbf{V_{gs}}$ values and sharing the common $\mathbf{V_{ds}}$ value (set as a variable). This will allow you to show all five curves on the same plot.

The MOSFET symbols use the convention where **source** and **drain** are the *top* and *bottom* terminals of the PMOS, respectively. In contrast, **drain** and **source** are the *top* and *bottom* terminals of the NMOS, respectively. Therefore, in order for your plots to match the conventions in the textbook, the source of the PMOS should be connected to Vdd (2.5V) and the source of the NMOS should be connected to ground.

Task 2: I-V Characteristics: Fixed Vds

After you do this, generate I_{ds}-V_{gs} curves for both the PMOS and NMOS transistor by sweeping $\mathbf{V_{gs}}$ over the range [-2.5 0] and a fixed $\mathbf{V_{ds}}$ of -2.5 V for the PMOS, and sweeping $\mathbf{V_{gs}}$ over the range [0 2.5] and a fixed $\mathbf{V_{ds}}$ of 2.5 V for the NMOS. This will ultimately lead to one plot for each transistor.

In an ideal transistor (Shockley), I_{ds} is 0 when $V_{gs} < V_t$. However, real transistors have subthreshold conductance. There are at least eleven different methods to determine threshold voltage from I_{ds}-V_{gs} data. You may use the constant current method to assume that any I_{ds} <= 0.1 uA * (W/L) constitutes an OFF device. Determine the threshold voltage for the NMOS and PMOS device.

What to Submit

As in lab 1, submit your designs and simulation results.