# CSCE 612
# Lab 2
# Characterization of AMI C5N Devices and Circuits
# Due Date: 2/21

## Introduction

As explained in Lab 1, SPICE/Spectre models have many parameters. However, these parameters can not be directly used to determine transistor performance information. This is why it is common for designers to run a series of device simulations when beginning to work with a new fabrication technology.

In this lab, you will use simulation techniques to determine behavioral characteristics for the NMOS and PMOS devices.

## Task 1: I-V Characteristics

In order to get Spectre to generate an I-V plot, you will need to perform a DC-sweep analysis. To do this, you will need one fixed DC source and one variable DC source.

The variable DC source is a regular DC source whose voltage is a simulation variable. Choose the variable name and specify this name in the voltage field in the **vdc** properties. In Spectre, add the variable by selecting Variables | Edit and enter the variable name with a value of 0. After this, add a DC Analysis, select "Design Variable" as the Sweep Variable, specify the variable name, and finally a start and end value. Select the drain terminal on the transistor to plot as a ***current*** output.

Generate $I_{ds}$-$V_{ds}$ curves for the NMOS and PMOS transistor by sweeping $V_{ds}$ over the range [0 2.5] and using fixed $V_{gs}$ values of [.8 1.2 1.6 2.0 2.4] for the NMOS and [-.8 -1.2 -1.6 -2.0 -2.4] for the PMOS (this will obviously require 5 separate simulations for each MOSFET). For the PMOS simulation, make sure you "decouple" $V_{ds}$ and $V_{dd}$ since the body terminal of the PMOS must be connected to a static DC source (supply) of 2.5 V.

The MOSFET symbols use the convention where **source** and **drain** are the *top* and *bottom* terminals of the PMOS, respectively. In contrast, **drain** and **source** are the *top* and *bottom* terminals of the NMOS, respectively. Therefore, in order for your plots to match the conventions in the textbook, the source of the PMOS should be connected to Vdd (2.5 V) and the source of the NMOS should be connected to ground. The variable DC sources should therefore be connected to the drain for both MOSFETs.

After you do this, generate $I_{ds}$-$V_{gs}$ curves for both the NMOS and PMOS transistor by sweeping $V_{gs}$ over the range [0 2.5] and using a fixed $V_{ds}$ of 2.5 V and fixed $V_{bs}$ of [-0.2 0.2]. In order to change $V_{bs}$, you'll need to use the 4-terminal version of the MOSFETs.

## Task 2: Threshold Voltage

In an ideal transistor (Shockley), $I_{ds}$ is 0 when $V_{gs} < V_t$. However, real transistors have subthreshold conductance. There are at least eleven different methods to determine threshold voltage from $I_{ds}$-$V_{gs}$ data. You may use the constant current method to assume that any $I_{ds}$ <= 0.1 uA * (W/L) constitutes an OFF device. Determine the threshold current for the NMOS and PMOS device.

**Task 3: Gate Capacitance**

Gate capacitance is voltage-dependent, but we can still obtain an effective capacitance averaged across the switching time.

Figure 1 shows an FO4 circuit that may be used to determine gate capacitance. Setup this circuit like you did in Lab 1, but this time the goal is to adjust $C_{delay}$ until the delay from c to g equals the delay from c to d. In this circuit, X3 and X6 have the same input slope and are of the same size, so when the delays are matched, $C_{delay}$ will have the same input capacitance as X4.

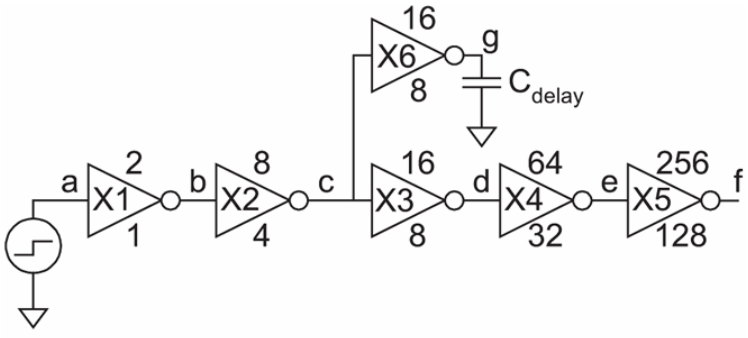


**Figure 1**

Once you determine $C_{delay}$, you must divide this value by the **total** gate width (in μm) contained within X4 to obtain the capacitance-per-micron of gate width ($C_{permicron}$). In order to set an initial (starting point) capacitance, refer to the gate capacitance estimation discussion in Chapter 2.

**In order to isolate gate capacitance, you must set the source and drain area and perimeter to 0 for the FETs in X3 and X6 in order to remove the effects of parasitic capacitance.**

**Task 4: Parasitic Capacitance**

Parasitic capacitance is the capacitance that is contributed by the source and drain. This includes gate-to-diffusion overlap and diffusion reverse-bias diode capacitance, as a function of diffusion area and perimeter (area is used for "vertical" diffusion diode capacitance; perimeter is used for the horizontal diffusion diode capacitance based on the thickness of the diffusion region). Like gate capacitance, this value is voltage-dependent. However, we can still estimate the average parasitic capacitance over the switching time.

Figure 2 shows a circuit that can be used to estimate these capacitances.

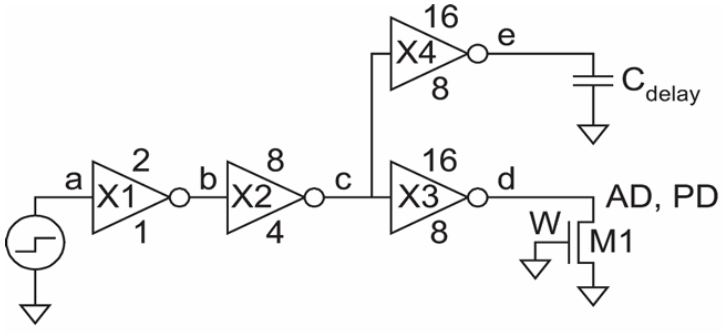

**Figure 2**

In this circuit, X3 drives the drain of an OFF transistor M1. This transistor's drain diffusion area (AD) and drain perimeter (PD) are computed automatically based on its channel width. X3 drives a capacitor whose value may be matched such that the delay of X3 and X4 are equal. This is the effective capacitance of M1's **drain**. Determine the capacitance per micron of width by normalizing the value of the width of M1. You may assume that the units per micron are the same for the source and the drain.

Repeat this test for the PMOS transistor. In this case, you'll need to reverse the direction of the PMOS and tie the gate voltage to $V_{dd}$.

## Task 5: Effective Resistance

Now that we have determined the per-$\mu$ gate capacitance $C_g$ and parasitic capacitance $C_d$ for the NMOS and PMOS, we can now estimate the resistance of $R_n$ and $R_p$ (for NMOS and PMOS) using the switch-level delay model. To do this, you may calculate the differences in delay for inverters with different fanouts.

In lab 1, you determined the rising and falling delay for a fanout-of-4 inverter. When you did this, you setup an inverter chain like the one shown in Figure 3.

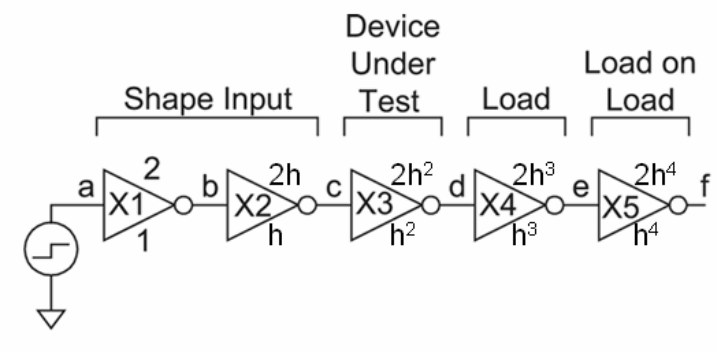


**Figure 3**

Figure 3 is more generalized than Figure 1 in Lab 1. Figure 3 shows a fanout-of-*h* inverter chain. In lab 1, $h=4$.

Assume X3 is pulling down. This yields the effective RC-model shown in Figure 4.

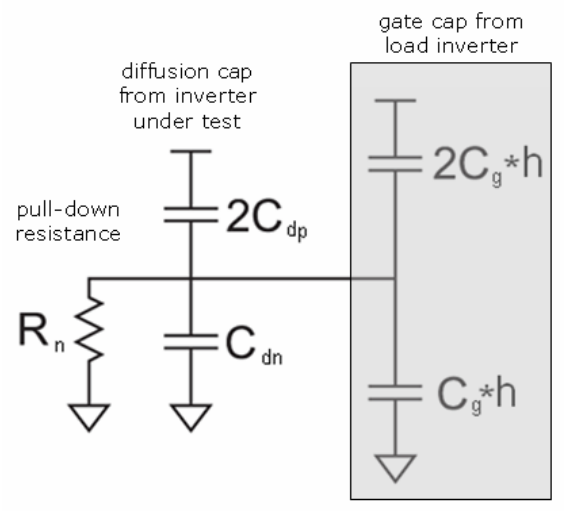


**Figure 4**

In this case, the delay may be calculated as $t = R_n * [(2C_{dp} + C_{dn}) + 3hC_g]$, where $C_g$ is the NMOS gate capacitance and $C_{d(n|p)}$ is the diffusion capacitance (representing the source terminal of the load inverter's PMOS and the drain terminal of the load inverter's NMOS).

Repeat your experiment from Lab 1, but this time measure the rise and fall times for the inverter-under-test's output (as opposed to the rise and fall *delays*). Next, adjust the inverter sizes over the entire design (internal FET widths) such that $h=3$. Once you do this, measure the rise and fall times for the inverter-under-test. Using the difference in these delays along with the gate and parasitic capacitance, you can use the following two equations to determine the effective resistance on the NMOS and PMOS in the ON state.

$$\Delta t_r = \frac{R_p}{2}\left(3 \cdot h_h \cdot C_g + C_{dn} + 2C_{dp}\right) - \frac{R_p}{2}\left(3 \cdot h_l \cdot C_g + C_{dn} + 2C_{dp}\right)$$

$$\Delta t_f = R_n\left(3 \cdot h_h \cdot C_g + C_{dn} + 2C_{dp}\right) - R_n\left(3 \cdot h_l \cdot C_g + C_{dn} + 2C_{dp}\right)$$

In these equations, $\Delta t_r$ and $\Delta t_f$ represent the difference in rise and fall delay, respectively. $h_h$ (=4) and $h_l$ (=3) represent the value of $h$ for the high-fanout and low-fanout, respectively. $C_g$ refers to the gate capacitance, and $C_{dn}$ and $C_{dp}$ refers to the parasitic capacitance for the NMOS (drain) and PMOS (source).

Use these equations to solve for $R_n$ and $R_p$.

**What to Submit**

As in lab 1, submit your designs and simulation results.