CSCE 612: VLSI System Design
Department of Computer Science and Engineering
University of South Carolina

This course is designed to tightly couple the teaching of VLSI system design fundamentals with a comprehensive, industry-standard IC design flow spanning tools from the three largest electronic design automation (EDA) vendors. By the end of the course, student design teams will work together to design a complete VLSI integrated circuit for fabrication in the AMI .5um process. The outcome of this process will serve to illustrate the way in which EDA tools manage the complexity of VLSI design and testing, from both a top-down and a bottom-up approach.

The course will be divided into four units. The first unit introduces MOSFET device fundamentals (physics, function, IC fabrication, etc.) and transistor-level CMOS logic design, layout, DRC, extraction, simulation, and verification. Using Cadence Virtuoso, students will design their own custom library of standard logic and memory cells in both schematic and layout form. They will test these circuits using Cadence Spectre. Next, they will learn how to characterize their cells using Cadence SignalStorm and specify this information as a Synopsys Design Compiler library as well as a Verilog behavioral cell library.

The second unit will introduce the students to digital system design through behavioral specification in HDL using the automated HDL design environment offered in Mentor's HDL Designer. The students will learn how to verify their designs using Mentor ModelSim as a behavioral simulation environment.

The third unit will require that students synthesize their HDL designs using Synopsys Design Compiler using the standard cell library and characterization information that they developed in the first unit. This unit will include meeting synthesis goals for area, timing, and power. This step will produce a Verilog cell-level netlist and an SDF cell delay model. These files will be combined with their Verilog behavioral cell library to be used for cell-level design simulation and timing verification in Mentor ModelSim.

In the final unit, students will use Cadence First Encounter to place-and-route their netlists using the layout versions of their standard cell library. After place-and-route,

they will extract parasitic RC information from their layouts to yield a combined cell- and wire-level timing model for final timing analysis in Mentor Modelsim. Finally, layouts from each design group will be combined using Cadence Virtuoso to form the complete chip layout which will be sent to MOSIS for fabrication.