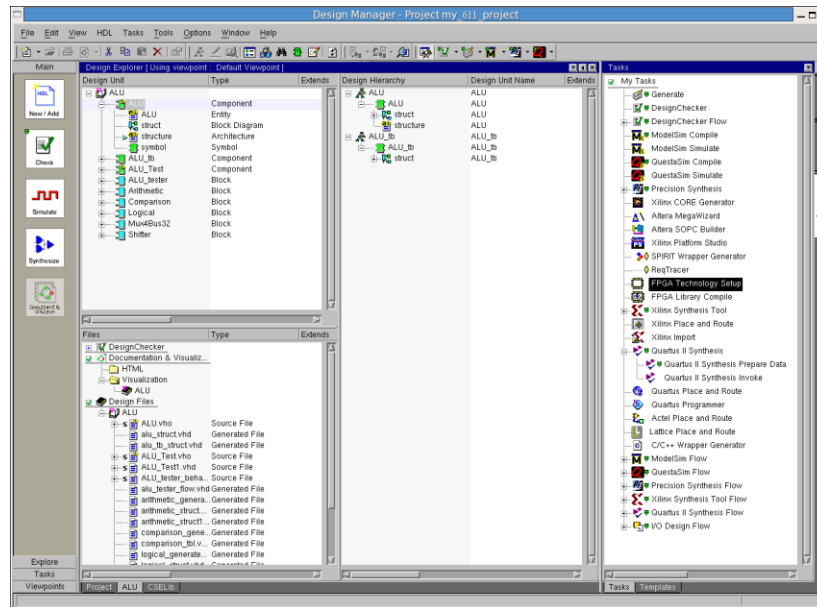


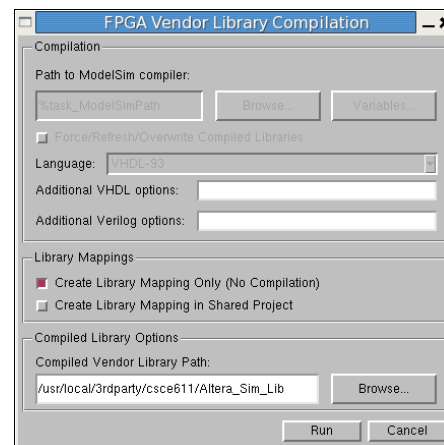
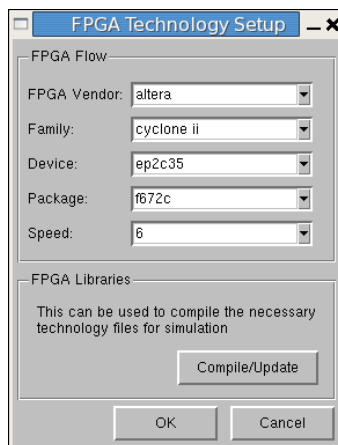
Post-Place-and-Route Simulation in Modelsim

Before FPGA verification of ALU design, we can simulate the placed and routed ALU design. A post-place-and-route simulation models interconnect delay, as well as gate delay. This type of simulation will most accurately match the behavior of the actual hardware. However, for large designs, it can take a significant amount of time to extract the interconnect delay values from the place-and-route information, and a significant amount of time to run the actual simulation.

In Design Manager highlight your ALU design, click the *Tasks/Templates* tab at the top right part of the window and double click the task *FPGA Technology Setup* from the *My Tasks* list.

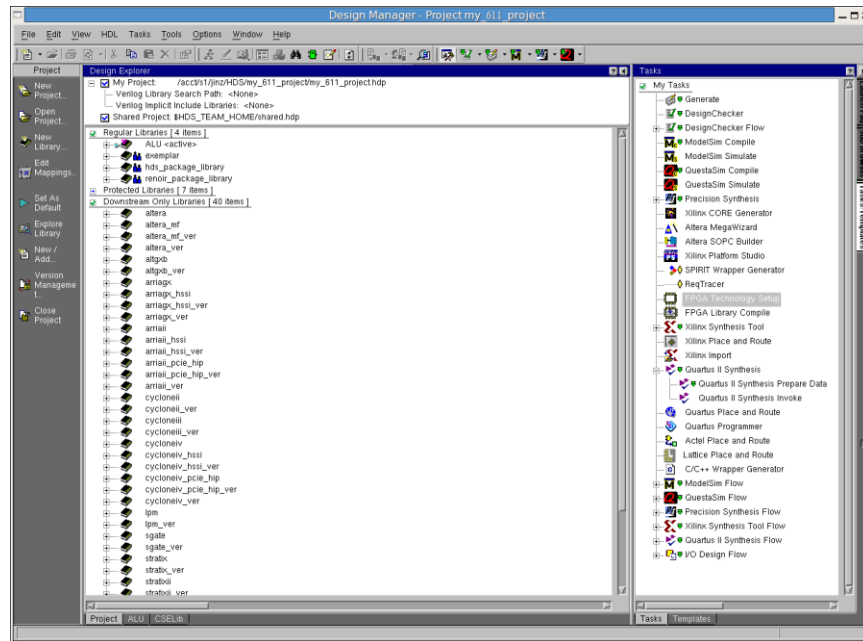


In the *FPGA Technology Setup* dialog box change the settings for the Altera Cyclone II EP2C35F672C6 FPGA.

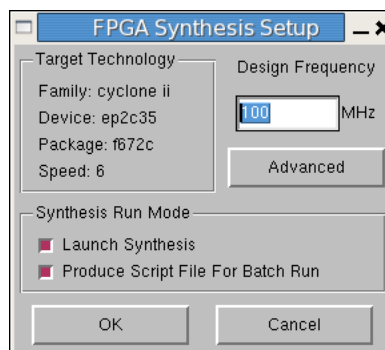


The next step is to setup the HDL Designer library mapping and compile options for simulation, access the related setup dialog box by pressing the *Compile/Update* button.

In the **FPGA Vendor Library Compilation** dialog box, unselect **Create Library Mapping in Shared Project**, select **Create Library Mappings Only** option, and set the compiled library path to “`/usr/local/3rdparty/csce611/Altera_Sim_Lib`”. Press the **Run** button to apply the options. Now these libraries are mapped as “downstream only” as they are used for simulation.



Switch to the **ALU** library view and highlight the **ALU** Component. Double click the task **Quartus II Synthesis** from the **My Tasks** list. After a moment, both a dialog box named **FPGA Synthesis Setup** and another one named **Log Window** pop up. Leave as default the settings in the **FPGA Synthesis Setup** dialog box and click the **OK** button.



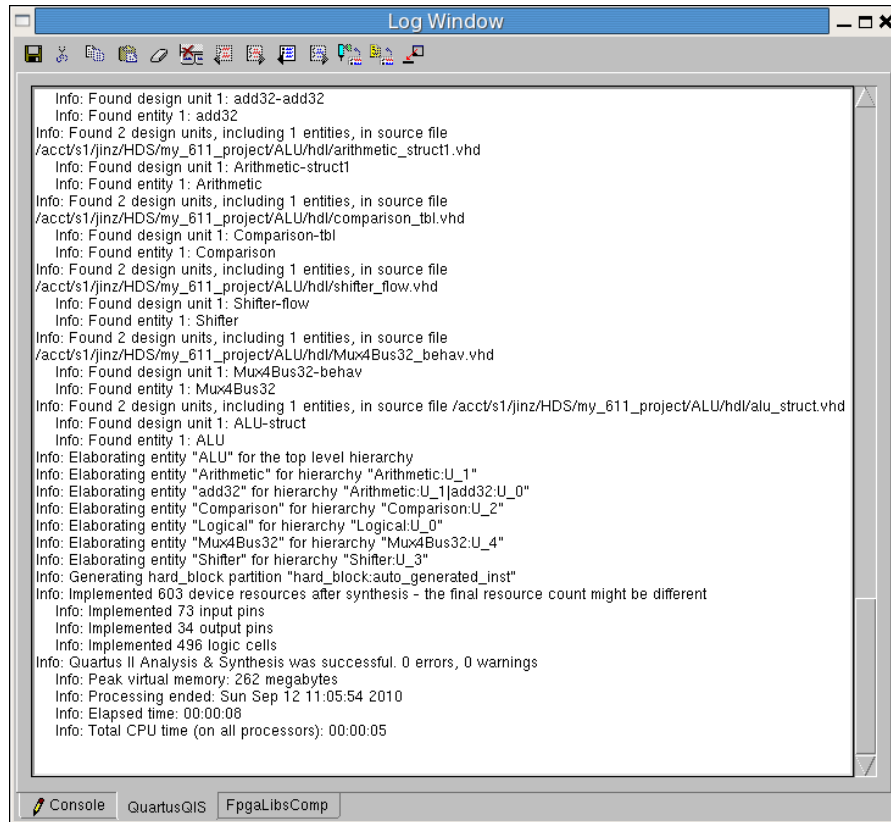
Now the **Log Window** shows the various synthesis steps being performed by Quartus II. The error messages, if any, would be reported at the end of the synthesis process. Please exam the error messages carefully.

Updates

If the **Log Window** shows the similar error message “Error Node instance “U_0” instantiates undefined “add32” file `/acct/s1/your_csce611_project_path/arithmetic_struct.vhd` Line 111”, go

to **Project** tab in **Design Explorer**, select **CSELib** in the **Protected Libraries**, right click it and select **Allow Analysis for Sim/Synth**.

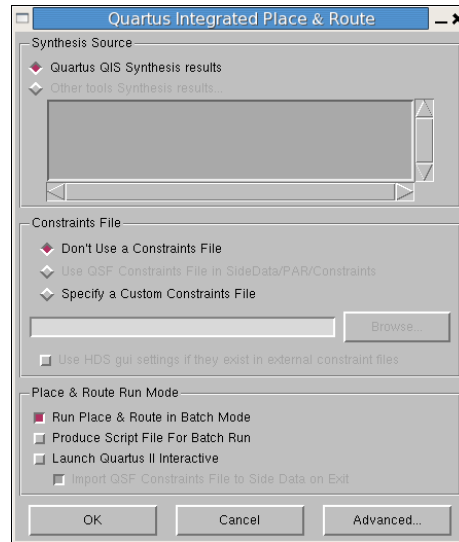
If synthesis is successful, Log Window shows the following message:



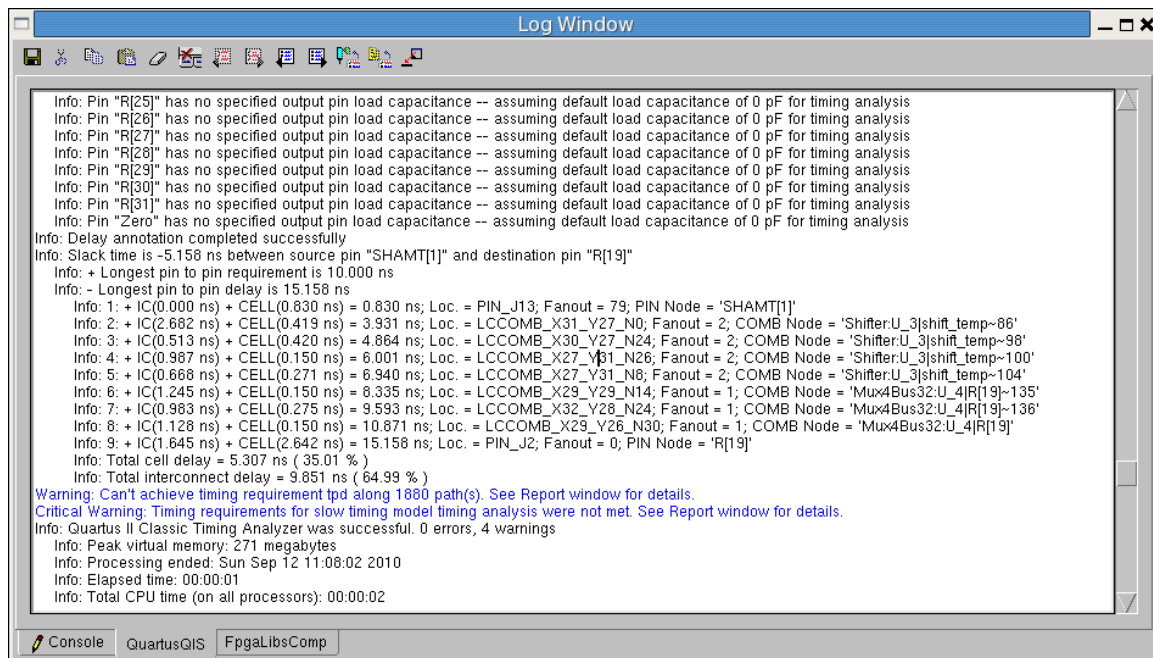
```
Log Window
Info: Found design unit 1: add32-add32
Info: Found entity 1: add32
Info: Found 2 design units, including 1 entities, in source file
/acct/s1/jinz/HDS/my_611_project/ALU/hdl/arithmetic_struct1.vhd
Info: Found design unit 1: Arithmetic-struct1
Info: Found entity 1: Arithmetic
Info: Found 2 design units, including 1 entities, in source file
/acct/s1/jinz/HDS/my_611_project/ALU/hdl/comparison_tbl.vhd
Info: Found design unit 1: Comparison-tbl
Info: Found entity 1: Comparison
Info: Found 2 design units, including 1 entities, in source file
/acct/s1/jinz/HDS/my_611_project/ALU/hdl/shifter_flow.vhd
Info: Found design unit 1: Shifter-flow
Info: Found entity 1: Shifter
Info: Found 2 design units, including 1 entities, in source file
/acct/s1/jinz/HDS/my_611_project/ALU/hdl/Mux4Bus32_behav.vhd
Info: Found design unit 1: Mux4Bus32-behav
Info: Found entity 1: Mux4Bus32
Info: Found 2 design units, including 1 entities, in source file /acct/s1/jinz/HDS/my_611_project/ALU/hdl/alu_struct.vhd
Info: Found design unit 1: ALU-struct
Info: Found entity 1: ALU
Info: Elaborating entity "ALU" for the top level hierarchy
Info: Elaborating entity "Arithmetic" for hierarchy "Arithmetic:U_1"
Info: Elaborating entity "add32" for hierarchy "Arithmetic:U_1|add32:U_0"
Info: Elaborating entity "Comparison" for hierarchy "Comparison:U_2"
Info: Elaborating entity "Logical" for hierarchy "Logical:U_0"
Info: Elaborating entity "Mux4Bus32" for hierarchy "Mux4Bus32:U_4"
Info: Elaborating entity "Shifter" for hierarchy "Shifter:U_3"
Info: Generating hard_block partition "hard_block:auto_generated_inst"
Info: Implemented 603 device resources after synthesis - the final resource count might be different
Info: Implemented 73 input pins
Info: Implemented 34 output pins
Info: Implemented 496 logic cells
Info: Quartus II Analysis & Synthesis was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 262 megabytes
Info: Processing ended: Sun Sep 12 11:05:54 2010
Info: Elapsed time: 00:00:08
Info: Total CPU time (on all processors): 00:00:05



Console  QuartusQIS  FpgaLibsComp
```

Next double click the task **Quartus Place and Route** from the **My Tasks** list. In the pop-up dialogue box named **Quartus Integrated Place & Route**, unselect **Produce Script File For Batch Run** and select **Run Place & Route in Batch Mode** under **Place & Route Run Mode**. Then click the **OK** button.

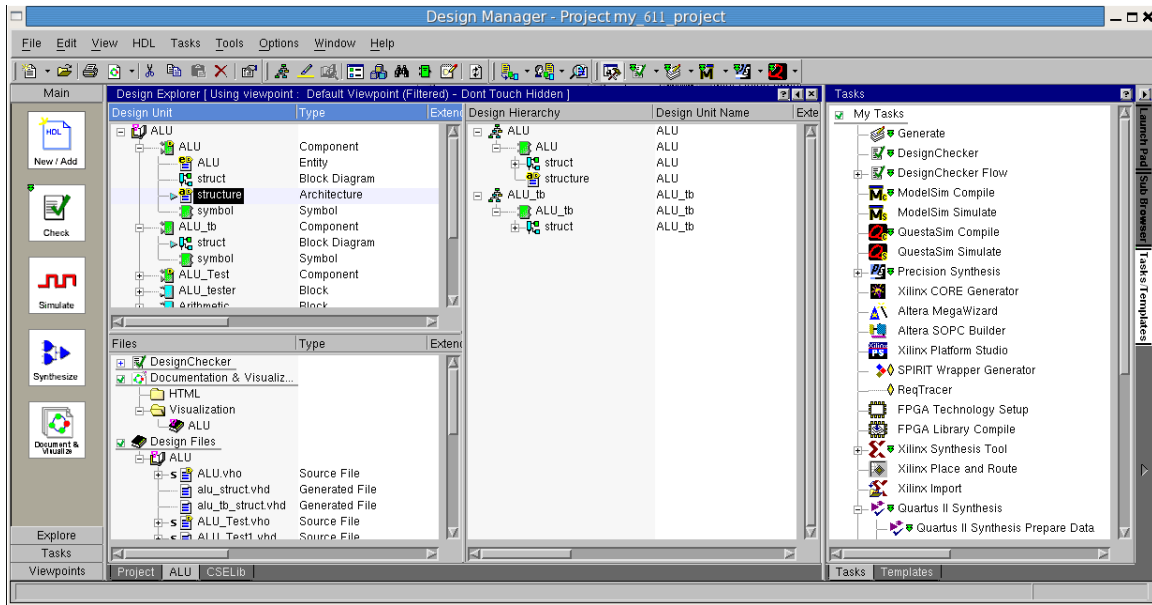


After Place & Route process is finished, Log Window shows the timing requirements were not met. This means the delay from ALU inputs to outputs is larger than 10 ns (1 / 100 MHz). According to the Timing report, the critical timing path in the ALU is 16 ns, which would be the shortest possible clock period if our ALU was used in a synchronous design.



In Design Manger click the  icon of the ALU Component and notice an overlay icon  is added to a newly-generated flat VHDL entity and architecture for the ALU, showing a new view for the ALU that is described by gate level views.

To set the gate level view as the default view, highlight the Architecture view named *structure* and right click on it and choose *set Default View*.



Finally launch the Modelsim simulator for post-place-and-route simulation. In the **Design Manager** highlight the **ALU_tb** component and click the ModelSim design flow button.

