

CSCE 313: Embedded Systems

Meeting times: Weekly lecture: M 3:55 to 5:35
Lab for Section 001: T 3:55 to 5:35
Lab for Section 002: W 3:55 to 5:35
Lab for Section 003: Th 3:55 to 5:35

First lecture: Monday, January 14
Last lecture: Monday, Apr. 29
Final exam: Monday, May 6 at 4:00 to 6:30
Class canceled: Monday, January 21 (MLK Day)

Locations: **Lecture:** Innovation Center, room 1400
Lab: Swearingen Engineering Center room 1D49 (1-4-5-2-3)
Will move to 3D22 sometime during the semester (5-1-2-4-3)

Textbook: Embedded Systems: ARM Programming and Optimization,
Elsevier (optional)
+ online materials available on <http://dropbox.cse.sc.edu>

Prerequisites: CSCE 211: Digital Logic Design
CSCE 212: Introduction to Computer Architecture
CSCE 240: Intro. to Software Engineering (**recommended:
you must be familiar with C++ and Linux**)

Bulletin Description:

Fundamentals of embedded systems: hardware components,
software components, hardware/software interface design, and
hardware/software co-design.

Instructor and Teaching Assistants:

Instructor: Jason D. Bakos
E-mail: jbakos@cse.sc.edu
Office: Storey Engineering and Innovation Center room 2213
Webpage: <http://www.cse.sc.edu/~jbakos>
Phone: 777-8627 (x7-8627)
Office hours: Monday, Tuesday 9:30 to 11:00

Teaching asst 1: Rasha Karakchi
E-mail: karakchi@email.sc.edu
Office: Storey Engineering and Innovation Center room 2236
Office hours: Tuesday, Wednesday 9:30 to 11:00
Available in lab Wednesday, 3:55 to 5:35

Teaching asst 2: James Coman
E-mail: jcoman@email.sc.edu
Office hours: Available in lab Wednesday, 3:55 to 5:35

Teaching asst 3: Dallin Williams
E-mail: dallinw@email.sc.edu
Office hours: Available in lab Tuesday and Thursday, 3:55 to 5:35

Electronic resources

1. Project submission, grade dissemination, up-to-date schedule, downloads, announcements, links to useful information, project descriptions, and recordings of all lectures are disseminated via the **CSE "Moodle" Dropbox**. (<http://dropbox.cse.sc.edu>)
2. We will use licensed electronic design software installed in the CSE departmental computer labs. The CSE labs are currently located in Swearingen 1D43 and 1D49. Partway through the semester we will move to the new lab in 3D22. Make sure you can log into the lab computers in 1D49.
3. We will also use DE2-115 FPGA project boards, located in the lab.
4. Urgent course announcements are broadcast on the website and to your **university e-mail** (@email.sc.edu). Please regularly check (or forward) this account.

Learning Outcomes:

Students will be able to:

1. Perform hardware/software co-design for a programmable embedded system;
2. Write software that directly interfaces with I/O peripherals such as LEDs, LCD panels, buttons, monitors, and remote consoles;
3. Write software that performs real-time processing of audio and video data;
4. Use high-level synthesis tools to develop coprocessor architectures in an embedded environment.

Grading structure

Lab 1: Lighting up the DE2 Board	10%
Lab 2: Image transformations and video out	10%
Lab 3: Performance analysis and code tuning	15%
Lab 4: Multiprocessor systems 1	15%
Lab 5: Multiprocessor systems 2	15%
Lab 6: High resolution, fixed-point fractal generation	15%
Final exam	20%

Grading scale:

A	90 ≤ score ≤ 100%
B+	85 ≤ score < 90%
B	80 ≤ score < 85%
C+	75 ≤ score < 80%
C	70 ≤ score < 75%
D+	65 ≤ score < 70%
D	60 ≤ score < 65%
F	score < 60

Academic Honesty Policy

Students are encouraged to assist their colleagues for the purpose of overcoming technical challenges related to the use of the design tools. Also, students working on a group project must (by definition) perform joint work. Any collaboration beyond these exceptions is prohibited and is subject to the university's guidelines, regulations, and policies regarding academic dishonesty.

See the USC Honor Code at bit.ly/USCHonorCode

Academic Honesty Policy (con't)

Any student caught committing an Honor Code violation will receive a grade of 0 for the corresponding assignment or exam and the instructor will report the violation to the Office of Academic Integrity.

Course Attendance Policy

Attendance in lecture and labs is optional but highly encouraged.

Group Work Policy

Group sizes of two are preferred and group sizes of one are allowed based on enrollment and hardware availability. Three-member groups are not allowed.

Choose your group partner wisely. Each of the partners in each group will receive the same grade for all labs.

Project Submissions

Submitted projects must compile (both hardware and software) to receive partial credit.

Each group must submit each project on Dropbox by 11:59PM on the due date.

Late projects will be charged a 10% grade penalty for each school day after the due date, limited to a maximum of 30%. This penalty is deducted from the raw graded score of the submission, so a one-day late submission earning a raw score of 80% will have a final score of $80\% \times 90\% = 72\%$.

At most, each group may only submit **one version** of any project; no resubmissions are allowed.

Students with Disabilities

Any student with a documented disability should contact the Office of Student Disability Services at 777-6142 to make arrangements for appropriate accommodations.

Syllabus Change Policy

This syllabus is a guideline for the course and is subject to change with reasonable advance notice.