

CSCE 313

Lab 4

Multiprocessor Image Transformation

Due Date: 3/25, 11:59pm

Design Requirements

The objective of this lab is to measure the performance impact of executing Lab 3 code on multiple processor cores.

Specific Tasks:

1. Add a second NIOS II/f processor, an on-chip memory, hardware mutex, and second floating point unit to your Platform Designer project.
2. Each processor core should share the DRAM, but make sure the linker confines the code to non-overlapping address ranges (see slides).
3. Change your Lab 3 code such that each processor computes half the rows of the transformed image using barriers to keep the processors synchronized between frames.
4. Measure the CPI of the fixed-point version of your rotation code.
5. Measure the overall speedup of the two-processor implementation as compared to the single-processor version.

Project Submission

Each group must submit a report that summarizes performance results.