

1. Assume a cache with the following characteristics:

Word size: 4 bytes
Block size: 16 words
Associativity: 4-way
Replacement policy: least-recently-used (LRU)
Total cache data capacity: 8192 bytes

- a. Assume the CPU uses a 32-bit address. Show how the address is split into **tag**, **index**, **word address**, and **byte address**.

- b. Show the final contents of the cache after the following series of accesses, where the address is shown in decimal. Assume the cache is initially empty.

4300, 10440, 16580, 18628, 6344, 2244

2. What is the average **memory access time** for the following system, which has a write-back cache:

Hit penalty: 10 ns
Miss rate: 2%
Probability that a cache line is dirty: 40%
Time required to fill a cache line: 100 ns
Time required to write-back a cache line: 200 ns

3. List and describe three reasons for a cache miss to occur.