Name (please print):_____ **Total points: ___/100**

Instructions
This is a CLOSED BOOK and CLOSED NOTES exam. However, you may use calculators, scratch paper, and the green MIPS reference card from your textbook. Good luck!

1. (Chapter 2/3, 10 points)

   Write a sequence of MIPS assembly code that will detect overflow for **signed subtraction**.

2. (Chapter 2, 10 points)

   Assemble the following instruction into hexadecimal representation:

   ```
   ADDI $2, $3, -8762
   ```

3 (Chapter 3, 20 points)

Assume the following floating-point format:

1 bit	5 bits	7 bits
sign	exponent bias=15	significand

a. What is the precision of this format?

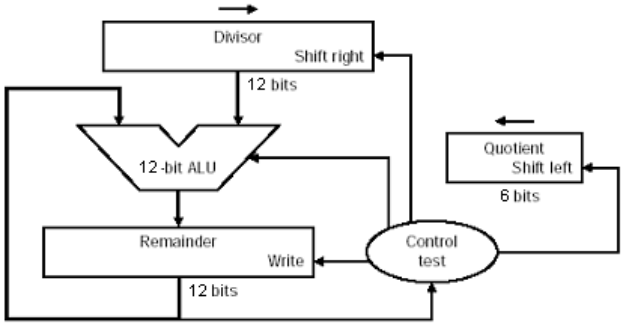
b. What is the range of this format?

c. Encode 16.62_{10} into this format (round down).

d. What is the rounding error of the value in this representation?

4. (Chapter 3, 10 points)

Assume the following divider design:



Assume the divisor and remainder registers are 12 bits and the quotient register is 6 bits. Give the values of each register for each step of the divide operation. You may use **decimal** or **binary** representation. Assume the divider is dividing **45** by **6** (assume all register values are unsigned).

Remainder Register	Divisor Register	Quotient Register

5. (Chapter 2, 20 points)

Translate the following high-level code to MIPS assembly. **`vals`** is an array of **half-words**:

```
i=0;
sum=0;
while (vals[i]!=0) {
      sum=sum+vals[i];
      i++;
}
```

6. (Chapter 2, 20 points)

Assume there is a MIPS pseudoinstruction named **`MERG16 rd, rs, rt`** that merges two register values by:

1. moving the low-order 16 bits of **rs** into the low-order 16 bits of **rd**, and
2. moving the low-order 16 bits of **rt** into the high-order 16 bits of **rd**.

Translate the following instruction into MIPS machine instructions:

```
MERG16 $2, $3, $4
```

Do not change the values of any registers except $1 (use for intermediate values) and $2 (the destination).

7. (Chapter 1, 10 points)

Assume you're the CEO of Intel Corp. and your design team tells you that they can increase the clock speed of your state-of-the-art processor from 3.0 GHz to 3.4 GHz, but in doing so the processor will go from being able to execute 4.2 instructions per clock cycle (on average) to 3.4 instructions per cycle. Is this a clock speed improvement a good idea or not? Why?