CSCE 613: INTRODUCTION TO CMOS VLSI DESIGN

1. CSCE 613: INTRODUCTION TO CMOS VLSI DESIGN

2. Credit: 3-hrs; Contact: 3 lectures of 50 minutes each or 2 lectures of 75 minutes each per week

3. Instructor: Jason Bakos

4. Textbook: Neil H.E. Weste, David Harris, CMOS VLSI Design: A Circuits and Systems Perspective 3rd Ed., Addison Wesley 2006, ISBN: 0321149017.

5. Specific Course Information
    a. Catalog Description: Design of VLSI circuits, including standard processes, circuit design, layout, and CAD tools. Lecture and guided design projects.
    b. Prerequisite: CSCE 211, ELCT 371 and by Topic: Digital logic, Electronics
    c. CSCE 5xx elective for computer science and computer information systems

6. Specific Goals for the Course
    a. LEARNING OUTCOMES: After completing this course students should be able to:
        1. *CMOS design:* Design CMOS logic using MOSFET devices, perform circuit-level simulation of CMOS logic gates to determine logic delay
        2. *Device characterization*: Characterize MOSFET devices for I-V behavior, gate and parasitic capacitance, and effective resistance
        3. *Standard cell design:* Design a library of standard logic, driver, and memory cells using schematic capture, layout, DRC, extraction, layout-vs-schematic, library characterization, and abstract generation
        4. *HDL design:* Design large-scale digital logic systems using VHDL behavioral design and simulation with a specific emphasis on synthesis to layout
        5. *Synthesis to layout:* Synthesize, place-and-route, and generate cell and interconnect delay models for VHDL designs using their custom-designed standard cell library
    b. For CE, CS, & CIS CSCE 613 is 5xx-level and therefore cannot be counted on to contribute to outcomes.

7. Topics Covered:
    - CAD/EDA design flow (spanning circuit-level, logic-level, and system-level)
    - Design methodologies and techniques
    - Logic delay and delay models
    - CMOS logic design
    - MOSFET semiconductor theory

- Circuit simulation
- Logic verification
- Standard cell library design
- Managing design complexity of large-scale digital systems
- Behavioral design of arithmetic logic unit (bit-wise logic, shifting, rotating, fast addition, fast subtraction, multiplication, division)

Class/Laboratory Schedule:
Lecture: 3 periods of 50 minutes or 2 periods of 75 minutes per week

Course Coordinator: Jason Bakos

Modification and Approval History:
Initial description April 1999
Revised, June 2001
Revised June 2005 by Caroline Eastman to modify format
Revised June 2005 by Jim Davis to modify textbook and content
Revised June 2011 by Jason Bakos to modify textbook and content