CSCE 612: VLSI SYSTEM DESIGN

Catalog Description:
612—VLSI System Design. (3) (Prereq: CSCE 211, 245) VLSI system design process models, introduction to EDA tools, HDL, modeling and simulation, logic synthesis and simulation, benchmark design projects.

Prerequisite(s) By Topic:
Digital logic
Programming in a high level language

Textbook(s) and Other Required Material:
Peter J. Ashenden, *The Designer's Guide to VHDL*, 2nd edition, Morgan Kaufmann Publishers, Inc., San Francisco, CA 2003.

J. Bhasker, *A SystemC Primer*, 2nd edition, Star Galaxy Press, Allentown, PA, 2004.

Computing Platform: Windows XP

Course Objectives: {Assessment Methods Shown in Braces}
1. <u>Modeling and Analysis</u>: Demonstrate the ability to analyze and create models of moderately complex digital electronics circuits and systems {tests, homework, project}
2. <u>Programming</u>: Demonstrate the ability to use hardware description languages (HDLs) as representation medium for expressing digital electronic design functionality and test bench functionality {tests, homework, project}
3. <u>Simulation Verification</u>: Demonstrate the ability to subject models of digital circuits and systems to simulation verification in terms of function and timing verification, and to plan and devise test scenarios for design verification {tests, homework, project}
4. <u>Design & Architecture</u>: Demonstrate the ability to use different architecture modeling styles (structural and behavioral), and to understand the differences of when to use each, as well as to demonstrate ability to reuse design units as components {tests, project}
5. <u>Requirements Specification and Design Planning</u>: Demonstrate the ability to follow specifications, to prepare deliverables according to requirements, and to devise test planning and time tracking/time management (task effort distribution) deliverables {homework, project}
6. <u>Project Execution and Reporting</u>: Demonstrate the ability to complete a significant VLSI design project having a set of objective criteria and design constraints {project}

Topics Covered:
1. Introduction to modeling and analysis using VHDL (2)
2. Data Types (2)
3. Control structures (2)
4. Composite data types and operations (1)
5. Additional modeling constructs (3)
6. Functions and procedures (3)
7. Packages (2)
8. Signal resolution and multi-valued logic (3)
9. Generics and parameterization (2)
10. Components and configuration (2)

11. File I/O (3)
12. Introduction to modeling and analysis using SystemC (4)
13. Class discussion of projects (10)
14. Reviews and examinations (3)

Laboratory Projects:
Students complete several laboratory design projects, including a major VLSI design project. One project is a moderately complex CPU control circuit, and the second project is a moderately complex arithmetic data path circuit.

Difference between Undergraduate and Graduate Work:
Graduate students work on the project by themselves rather than in teams of two and are also graded on a more rigorous scale (exams), and are given additional assignments (homework).

Syllabus Flexibility: High. Choice of textbook and design project determined by instructor

Relationship of Course to Program Outcomes:
The contribution of each course objective to meeting the program outcomes is indicated with the scale:
3 = major contributor, 2 = moderate contributor, 1 = minor contributor. Blank if not related.

Course Objectives	Program Outcomes										
	1. Logic & Math	2. Computing Fundamentals	3. Apply Computing Principles	4. Work on teams	5. Communicate Effectively	6. Liberal arts & Soc. Sciences	7. Basic Science and Lab Procedures	8. Learn New Tools & Processes	9. Employed upon Graduation	10. Application Area	11. Electronics and Digital Sys Design
1. Modeling and analysis	2	1	2					3	2	1	3
2. HDL Programming		2	2					3	1		2
3. Simulation verification			1	1			1	3	1		3
4. Design and architecture				1				1	2		3
5. Requirements specification and design planning				1	1				2	2	1
6. Project execution and reporting				1	1		1		2		1

Estimated Computing Category Content (Semester hours):

Area	Core	Advanced	Area	Core	Advanced
Algorithms			Data Structures		
Software Design		1	Programming Languages		
Computer Architecture		2			

Estimated Information Systems Category Content (Semester hours):
Computer Information Systems majors do not take this course.

Oral and Written Communication:
Documentation for major VLSI design project, comprised of a project report, testing and simulation results, effort distribution data (task breakdown)

Social and Ethical Issues: None

Theoretical Content: None

Analysis and Design:
Significant VLSI design project

Class/Laboratory Schedule:
Lecture: 3 periods of 50 minutes or 2 periods of 75 minutes per week

Course Coordinator: Jim Davis

Modification and Approval History:
Initial description, March 22, 1999
Revised, June 2001
Revised, June 2005 by Jim Davis to update textbook and content