New topuc: Moltiplexers, Decoders, and Programmebly Note Title Sate input Lagre Devices Multiplexer, and Deraden ave examples of medium-scale integrated 2-to-1 MUX which contract 12-100 Ζ gates in one peckage A Gutral input (one chip). LSI (Large-sude integrated) Figure 9-1: 2-to-1 Multiplexer and Switch Analog civerits: ~100 - severethousand, VESI: from several thousand up A mithelexer (MUX) is also colled a date scleator, Z= A'IG+AI,



Figure 9-3: Logic Diagram for 8-to-1 MUX



## CSCE211, Homework Assignment No. 5

	· Show all your steps—answers alone are not sufficient.
	· Homework must be done neatly
	· Use straight-edged paper (no notebook tear-outs with ragged edges)
	• STAPLE papers to a signed cover sheet.
	Please print the following for reference and for this assignment: MUX-Decoder instructions. Also, please
	print for reference and inclusion in your Homework paper MSI diagrams 74LS151 (8-to-1 MUX) and
	74LS138 (3-to 8 Decoder/De-MUX)
	1. Use a 74x151 (8-to-1 MUX) to implement $f(W, X, Y, Z) = Sm(2, 4, 7, 8, 9, 13, 14)$ . Use the "rowpairs"
	method shown in class. Show all enable and address connections. (20pts) (See instructions
	above.)
	2. Use a 74x138 decoder and an external AND gate to implement $f(X, Y, Z) = Sm(1, 2, 4, 5, 6)$ .
	Show all enable and address connections. (HINT: AND the MAX terms) (20pts) (See instructions
	above)
	3. Use a 74x138 decoder and an external NAND gate to implement $f(p, q, r) = Sm(1, 3, 7)$ . Show all
	enable and address connections. (20 pts) (See instructions above)
	4. Design an 8-to-1 MUX from three 4-to-1 MUXs. Label the inputs on each 4-to1 MUX as I0 to I3.
	In the "first stage," place one MUX on "top" of another and connect their select lines S1 (most
	significant) and S0 together. Let I0 on the "top" MUX correspond to D0 of 8 inputs and let I0 on the
	"bottom" MUX be D4. Use the third MUX to select between the two "first-stage" MUX outputs. You
	can configure a 4-to-1 MUX to be a 2-to-1 MUX by setting its MS select line to logic "0." When you
_	finish, label the three 8-to-1 select lines as S2 (most significant) to S0 (least significant). (20 pts)
	5. Design an 8-input to 8-output MUX-DEMUX system using a 74x151 for the MUX part and a
	74x138 for the DEMUX. Leave the outputs of the 74x138 as active-low signals (leave the output
	bubbles as-is). Configure ("hard wire") the select-lines values on the MUX and address-lines values on
	the DEMUX so that <i>input</i> D4 is routed to <i>output</i> Y6_L. Wire so that there is only <b>one</b> active low
	ENABLE signal that controls <b>both</b> chips. You can do this because there are 3 enable lines (one active
	high, two active low) on the DECODER (20pts).
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742151 EN-L: emple low: emples when o EN\_L (7) kisubles when C D0 (4) S2istu most significant (MS) control but S0 is the least significant (LS) control but K D1 (3) D2 (2) DO-DFane the data inputs C D3 (1) Y is the acgosted output ► D4 (15) ► D5 (14) 74x151 Check: what is Y when D6 (13) S0 (LS) - EN-L =0 S2 (MS) D7 (12) D7 - SØ=Sl=SZ=1? so<sup>(11)</sup> S1 (10) the Motoro la datasheet, which is linked to the course web sole. Note that it provides a trill table on uses different nones for the variable,

5. Design an 8-input to 8-output MUX-DEMUX system using a 74x151 for the MUX part and a 74x138 for the DEMUX. Leave the outputs of the 74x138 as *active-low* signals (leave the output bubbles as-is). Configure ("hard wire") the select-lines values on the MUX and address-lines values on the DEMUX so that *input* D4 is routed to *output* Y6\_L. Wire so that there is only one active low
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