Proposed Seminar Outline: Tsinghua University

Dr. James P. Davis
University of South Carolina
Columbia, S.C., U.S.A.

Session 1: High-level VLSI Digital Systems Design – Methods, Notation, Architecture

Abstract: In this session, we explore issues and methods for the analysis, architecture and design of computing systems implemented in VLSI circuits. We focus on the high-level engineering of such systems, starting with systems analysis, and targeting the systems design to custom-logic and programmable logic VLSI devices. We'll use the *Executable ASM* (Algorithmic State Machine) method and notation to capture high-level designs, comparing this approach to HDLs such as VHDL, and systems-level description languages such as SystemC.

1. Introduction to High-level Design (50 minutes)
    - 1.1 Rationale – Design Issues and Trends
    - 1.2 Systems – Custom Logic versus Microprocessor Embedded
    - 1.3 Concepts – Design Hierarchy, Modeling, Abstractions, Patterns, Reuse
    - 1.4 Process – Design Objectives, Planning, Activities
    - 1.5 Methods 1 – Design Representation and Search Space
    - 1.6 Methods 2 – Model-Driven Architecture (MDA) for VLSI Systems
    - 1.7 Metrics – Measuring Effectiveness and Productivity

    Question & Answer

2. Teaching & Practicing High-level Design (70 minutes)
    - 2.1 Using the Executable ASM Method
    - 2.2 Architecture of Digital Systems – Control and Datapath
    - 2.3 Analysis and Modeling of Algorithms and Protocols
    - 2.4 Datapath-Dominated Designs – Arithmetic and Filter Circuits
    - 2.5 Control-Dominated Designs – Protocol Engines
    - 2.6 Applying Architecture Patterns for Reuse

    Question & Answer

3. Example High-level System Designs (50 minutes)
    - 3.1 Unsigned Integer Multiplier Circuits
    - 3.2 MAC Layer for 802.11b Wireless LAN

    Question & Answer

4. Session Wrap-Up

Proposed Seminar Outline: Tsinghua University

Dr. James P. Davis
University of South Carolina
Columbia, S.C., U.S.A.

Session 2: VLSI Digital Design – Methods for CMOS Microelectronics and Nanoelectronics Systems-on-Chip (SoC)

Abstract: In this session, we explore the issues and methods for the analysis, architecture and design of computing systems, by looking at the device technologies for custom logic and programmable logic devices. In particular, we examine the design issues for CMOS VLSI systems with requirements for highly integrated digital circuits that are high-performance and low power consumption. In addition, we examine how to consider low-level design issues when doing high-level ASM design and architecture analysis. Finally, we discuss some of the issues for VLSI systems design for next generation nano-electronics technologies that will be available within the next 5-8 years.

1. Introduction to CMOS-level Design (40 minutes)
    - 1.1 Rationale – Design Issues and Trends
    - 1.2 Devices – Custom Logic versus Programmable Logic
    - 1.3 Concepts – Design Hierarchy, Models, Libraries, Reuse
    - 1.4 Process – Design Objectives, Planning, Architecture, Synthesis, Layout
    - 1.5 Methods – Design Representation, Bridging High-level & Low-level Design

    Question & Answer

2. Teaching & Practicing Low-level CMOS VLSI Design (60 minutes)
    - 2.1 The Switch Model – Its Relationship to Gate-level and Register-level Design
    - 2.2 CMOS Architecture – Device Units and Interconnect
    - 2.3 CMOS Systems Analysis – Transistors, Inverters, Wire Modeling, Parasitics
    - 2.4 CMOS Layout for Custom Logic – the "Sea of Gates" Mapping Model
    - 2.5 Using CMOS-based Programmable Logic Devices

3. Some Integrated High-level/Low-level Design Examples (40 minutes)
    - 3.1 Model-Driven Architecture (MDA) Using Executable ASM Models
    - 3.2 Designing for Custom Logic
    - 3.3 Designing for Programmable Logic

    Question & Answer

4. Introduction to Nanoscale Electronics Systems Design (40 minutes)
    - 4.1 Nanoelectronics versus CMOS Microelectronics Design
    - 4.2 Types of Nanoelectronics Device Substrates
    - 4.3 Nanocomputing – Design and Architecture Issues

5. Session Wrap-Up