



## USC NanoCenter Symposium V

### Exploring Nano-Computing: Building Computing Systems On Nanoscale Semiconductor Devices

Dr. James P. Davis, Associate Professor  
Department of Computer Science and Engineering  
University of South Carolina  
Columbia, SC 29208 USA  
[jjmdavis@cse.sc.edu](mailto:jjmdavis@cse.sc.edu)

#### Extended Abstract

For 30 years, we've been computing on semiconductors whose growth in density conforms to Moore's Law--the capacity of devices doubles every 18 months. This "law" has held to current generations of devices, and should hold through 2010-2015 (by some accounts). However, increasing complexity and design packaging densities with smaller feature geometries brings great stress to the design community. This community is currently focused on these issues, not on the coming molecular-level nanoscale revolution.

How will we build large-scale, reliable computing systems using molecular nanoscale electronics? We believe this is a question of significant importance that is being largely ignored by the Nano-community. Having solved the problems of fabricating nanoscale devices and circuits without understanding how we will use them to build Nano-Computers is like "being all dressed with no place to go". To wit, our research involves investigating the following sub-topics essential for answering the broader question of "wither Nano-computing":

(1) What kinds of computing systems and applications will we construct on nanoscale substrates? The current computing paradigm, many researchers believe, should hold well into the nanoscale, as we currently have 90nm CMOS devices and the industry is pushing towards devices with line widths of 35-40 nm. Constructing computing architectures on CMOS devices would continue, as these densities grow from tens-of-millions to tens-of-billions of transistors. However, articulating the types of systems possible on a molecular nanoscale substrate is an open question. There are computational algorithms not solvable in realistic terms (time and resource usage) that may be more efficiently solvable on nanoscale computing structures employing massive fine-grained parallelism. Our research is exploring classes of algorithms, their complexity functions, and their realization on massively parallel architectures suitable for nanoscale devices. Much of this is related to the notion of employing architecture "patterns" of differing scope and complexity.

(2) How will algorithms/applications/systems be designed? Higher-level abstractions are required to formalize large-scale systems. Research shows that "design units", the components that can effectively be managed by a single VLSI logic designer, tend to cluster effectively around a size of 50,000 CMOS gates. Larger systems are then constructed of such units, where the largest and most complex semiconductor device--the Intel Pentium® 4 microprocessor--contains approximately 45 million transistor gates. Researchers are working on platform-based design approaches to allow larger design units to be manageable, building them from smaller reusable design units. Our research is looking at this current trend, and exploring which deep sub-micron design paradigms are likely to yield effective results at the molecular nanoscale. In addition, we are looking at more effective means to take arbitrary system applications, subject the analysis of these to appropriate system-level design methods, and effectively organize them for efficient implementation on nanoscale substrates.

(3) How will we insure functional integrity in the face of declining yield? Circuit yield is likely to be dynamic, changing on a given device over time, on nanoscale substrates, as they are more sensitive to noise and disruption as a result of atomic particle collisions. This requires that nanoscale designs be "adaptive" and "reconfigurable" in the face of unpredictable degradation. Reconfigurable devices such as today's FPGAs are used to study yield degradation in harsh computing environments for "rad-hardened" applications. In addition, there are a number of results in adaptive design techniques for high-reliability and high-availability VLSI devices, using various test techniques in the design of combinational and sequential logic systems. We are beginning an investigation of requirements for constructing "self-aware" logic architectures, using reconfigurable computing and built-in testing schemes employed in today's logic design methods as a basis for studying this important problem.