



Design Test Case Worksheet Computer Engineering Design Lab/Project (for use in CSCE courses 313/491/611/612/613)

Instructions: For each test case scenario, fill in one row in the table. Number each test case. Give each one a meaningful test name. For each case, indicate as precisely as you can, (1) the input signal/bus/register/memory set-up to trigger your test, and (2) the expected results of your test run, in terms of bus/signal/register/memory values you should see, and on what simulation clock cycles you expect to see these values (if relevant). The simulation clock cycle should be indicated for intermediate values, or when you are watching an output bus change value multiple times during a single test run. These fields get filled out **before** you execute the simulation run. The field for observed description of the simulation run results is filled in **after** you simulate. This should describe the overall results. This would provide a narrative that goes along with the simulation output—waveforms or screen dumps of simulator results.

Test No.	Test Name	Simulation Input			Expected Results			Observed Outcome (in text)
		Elapsed Cycle #	Input Bus Name	Value	Elapsed Cycle #	Bus Name	Value	