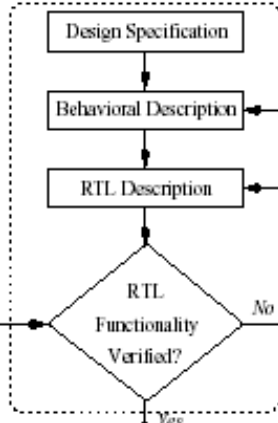


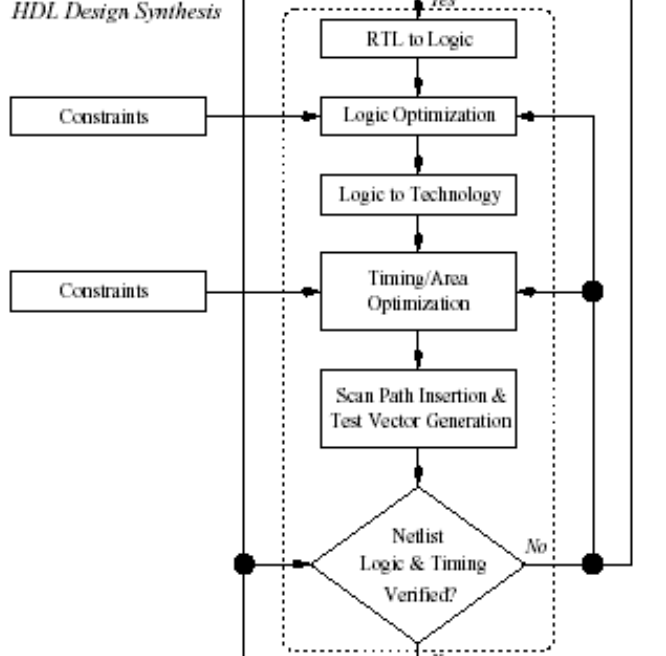
CSCE 612: Digital Design Using VHDL: DESIGN FLOW CHART

HDL Design Capture



VHDL / Verilog

HDL Design Synthesis



1. Modelsim (VHDL / Verilog)
 2. Synopsys
 - VHDL (Scirocco & Virsim, VSS)
 - Verilog (VCS & Virsim)

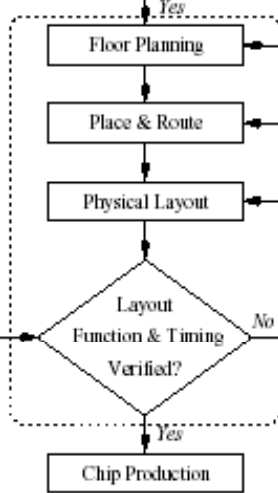
VSS: VHDL system simulator
VCS: Verilog Simulator

Synopsys: Design Compiler

Synopsys: PrimeTime Timing Analyzer

Synopsys: VERA
Test bench automation tool

Design Implimentation



Xilinx: ISE

2. Setting up the environment

1. Source the .cshrc file, after typing in the following commands in the file
 - source /etc/cshrc
 - source /usr/global/etc/synopsys.csh
 - source /usr/global/etc/modelsim.csh

3. Tools

(A) Modelsim

(a): Compiling the design

- Create the directory, then copy all of the VHDL files to this new directory
- Make sure the new directory is the current directory by selecting **File > Change Directory** (Main window).
- Start ModelSim with one of the following:
for Windows - your option - from a Windows shortcut icon, from the Start menu, or
from a DOS prompt:
modelsim.exe
- Before you compile any HDL code, you'll need a design library to hold the compilation results. To create a new design library, make this menu selection in the
Main window: **File > New > Library**.
Make sure **Create: a new library and a logical mapping to it** is selected.
Type "work" in the Library Name field and then select **OK**.
- Compile the file *counter.vhd* into the new library by selecting **Compile > Compile**.

(b): Loading the design

- Load the design unit by selecting **Simulate > Simulate**.
- Next, select **View > All Windows** from the Main window menu to open all ModelSim windows.
(PROMPT: view *)
- Next let's add top-level signals to the Wave window by selecting **Add > Wave > Signals in Region** from the Signals window menu.
(PROMPT: add wave /counter/*)

(c): Running the simulation

- Click in the Main window and enter the following command at the VSIM prompt:

force clk 1 50, 0 100 -repeat 100

ModelSim interprets this **force** command as follows:

- force clk to the value 1 at 50 ns after the current time
 - then to 0 at 100 ns after the current time
 - repeat this cycle every 100 ns
- **Run**. This causes the simulation to run and then stop after 100 ns.
(PROMPT: run 100)
 - **Run -All**. This causes the simulator to run forever. To stop the run, go on to the next step.
(PROMPT: run -all)
 - Select the **Break** button on either the Main or Wave toolbar to interrupt the run. The simulator will stop running as soon as it gets to an acceptable stopping point and step through your design