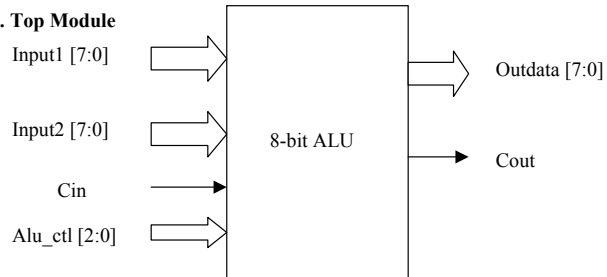


**CSCE 612- Digital Design Using VHDL**  
**Homework #4**  
 2/3/2003

**1. Top Module**



**2. Alu\_ctl**

Mnemonic	Alu_ctl	ALU Function
ADD	000	Input1 + Input2
SUB	001	Input1 - Input2
OR	010	Input1 OR Input2
AND	011	Input1 AND Input2
NOT	100	NOT Input1
EXOR	101	Input1 XOR Input2
EXNOR	110	Input1 XNOR Input2

**3. Sub Modules**

Design a 4-bit ALU block and instantiate it twice to realize an 8-bit ALU. The reason behind doing this is to practice bottom-up design, wherein we partition a big design into manageable smaller blocks. Design and test each of the sub blocks individually and finally integrate all the sub blocks. This practice will reduce the complexity of the design. From the optimization point of view, this approach will give the tool more room to optimize the design and place and route the design effectively.

