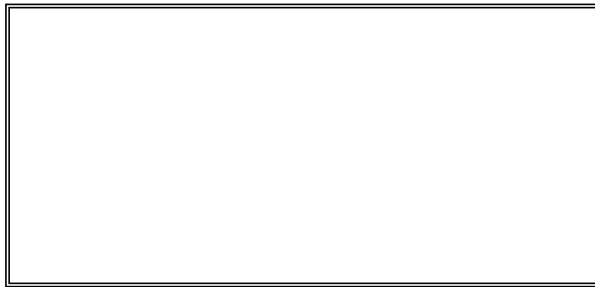


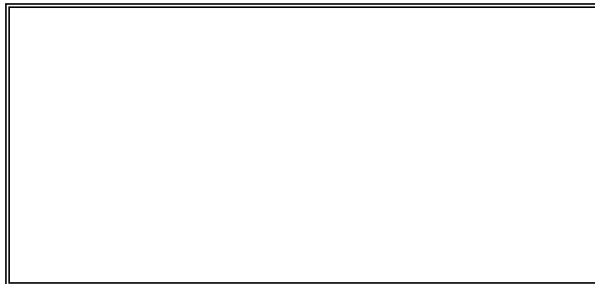
# Modeling a 3:8 Decoder-2

Figure source: Tanenbaum © 1999 Prentice Hall Publishing

A functional model of the Decoder, using Boolean expressions:

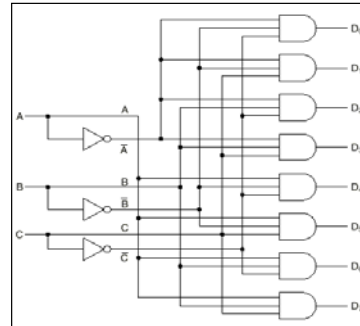


A behavioral model of the Decoder, using conditional assignments:



## 3:8 Decoder – HW#3:

- ✓ How would we model the Decoder operation using a functional style of VHDL assignment?
- ✓ How would we model the same operation using a behavioral style of assignment?
- ✓ WRITE YOUR ANSWER HERE & TURN IN.



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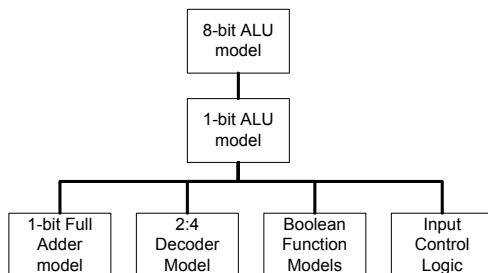
# Modeling an Arithmetic Logic Unit-5

Source: Tanenbaum, 4<sup>th</sup> ed. © 1999, Prentice-Hall

F <sub>0</sub>	F <sub>1</sub>	ENA	ENB	INVA	INC	Function
0	1	1	0	0	0	A
0	1	0	1	0	0	B
0	1	1	0	1	0	$\bar{A}$
1	0	1	1	0	0	$\bar{B}$
1	1	1	1	0	0	A + B
1	1	1	1	0	1	A + B + 1
1	1	1	0	0	1	A + 1
1	1	0	1	0	1	B + 1
1	1	1	1	1	1	B - A
1	1	0	1	1	1	B - 1
1	1	1	0	1	1	-A
0	0	1	1	0	0	A AND B
0	1	1	1	0	0	A OR B
0	1	0	0	0	0	0
0	1	0	0	0	1	1
0	1	0	0	1	0	-1

## The assignment for HW #4:

- ✓ Create the hierarchical model for the 8-bit ALU, using the hierarchy as shown here.
- ✓ Use Entity/Architecture pairs for each component level.
- ✓ Use component instantiation and port maps to define the binding between levels in the design hierarchy.
- ✓ You need to be careful about when to use structure (E/A pairs) and when to use functional grouping (as in concurrent assignments and process blocks).
- ✓ Generate the 16 different simulation runs with waveform output, for each of the four functions, plus the different input control functions, corresponding to the ALU's truth table.



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