

CSCE 612

Digital Design using VHDL

Spring 2003 – MWF 11:15-12:05 – SWGN 2B11 (300 S. Main St.)

Course Description: Language-based design of digital systems has become the predominant means of realizing systems design for VLSI in a wide range of custom logic applications. VHDL has been in use for more than a decade and millions of lines of systems code has been written using the language to model and synthesize circuits for every conceivable application. In this course, we will focus on the acquiring of skills necessary to model digital systems—both combinational logic and sequential logic—using VHDL as the medium for representing the designer’s intent. We will use language-based simulation as a means to explore the completeness and correctness of the models so created.

Course Outline & Topics:

The following revised outline has been devised for the course, based on a number of factors (see the course web page for more details).

1. Roth – Chapter 1 – Overview of VHDL as a modeling medium.
2. Roth – Chapter 2 – Diving into VHDL and system modeling.
3. Ashenden, Chapter 1 – Backing up: Starting with pedagogy of the Language (Lexical, Syntax, Semantics).
4. Ashenden, Chapter 2 – Data Types.
5. Ashenden, Chapter 3 – Control Structures.
6. Ashenden, Chapter 4 – Composite Data Types & Operators.
7. Ashenden, Chapter 5 – Additional Modeling constructs (hierarchy, component instantiation, etc.)
8. Ashenden, Chapter 7 – Functions & Procedures.
9. Ashenden, Chapter 8 – Packages.
10. Ashenden, Chapter 11 – Signal Resolution & Multi-valued Logic
11. Ashenden, Chapter 12 – Generics & Parameterization.
12. Ashenden, Chapter 13 – Components & Configuration.
13. Ashenden, Chapter 18 – File I/O.
14. Roth – Chapter 4 – Models of Arithmetic Circuits.
15. Ashenden, Chapter 6 – Arithmetic Modeling – the Pipelined Multiplier Accumulator.
16. Roth – Chapter 6 – Overview of FPGAs.
17. Roth – Chapter 8 (sections 8.8, 8.9) – VHDL for Logic Synthesis.

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Office Hours: By appointment.

Texts:

1. Roth, Charles H., [*Digital Systems Design Using VHDL*](#), PWS Publishing Inc., Boston, MA, 1999.
2. Ashenden, Peter J., [*The Designer's Guide to VHDL*](#), Morgan Kaufmann Publishers, Inc., San Francisco, CA, 1996.

Grading Policy:	<i>Homework:</i>	15%
	<i>Examinations (3):</i>	60%
	<i>Design Projects (#1, #2):</i>	25%