

CSCE 313

Embedded Systems Programming

2003/2/3

Spring 2003 – Lecture 9

M68000: Signals and Handshaking

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Some figures: G. Kane © 1981 Prentice Hall Publishers, Inc.
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Lecture 9 - Outline

● Objectives.

- ✓ Understanding of basic elements of the 68000 architecture:
 - ✦ Signals to/from the CPU to memory and peripherals.
 - ✦ Bus Structure.
 - ✦ Signaling Handshaking between CPU, Bus and Memory/Peripherals.
 - ✦ We'll use our understanding of the signals and the basic structure of the interactions between CPU, bus resources, and modules located on the bus.
 - ✦ Since M68000 has linear address space, and is fully memory mapped I/O, there is a single bus for memory and peripheral access. (Other processors, such as Pentium and later versions of 68000, have separate bus architectures for each).

● Concepts.

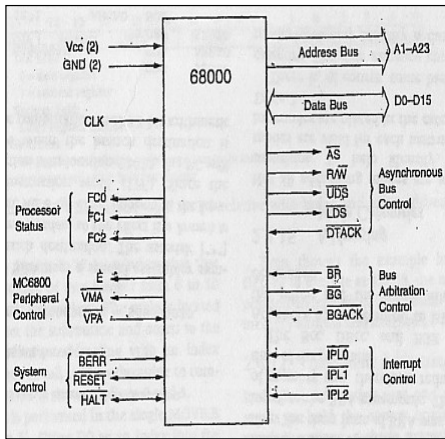
- ✓ Buses
- ✓ Control Signals
- ✓ Handshaking protocols
 - ✦ Memory access
 - ✦ Peripheral access
 - ✦ Bus timing
- ✓ Source: MacKenzie, Chapter 2, pp. 69-77.

M68K Architecture – Signals and Buses

Source: MacKenzie © 1995 Prentice Hall Publishers

● Address Bus (A0-A23)

- ✓ Unidirectional: CPU writes and address onto this bus, & other modules read & decode its value.
- ✓ Pin A0 is special: it is used to select an even or odd byte when "byte mode" data operation is specified.
- ✓ Pins A1-A23 (for the 24 bit memory address) is always aligned on even byte boundary (because there's no "1" in LSB of address word).



Data Bus (D0-D15)

- ✓ Bi-directional: can be written to and read by the CPU and other bus "modules".
- ✓ Two modes: (1) data: transferring byte or word data for each bus cycle; (2) interrupt mode: on the Acknowledge cycle for an "interrupt" of the CPU, the Interrupt Vector # is placed on D0-D7 (possible 8 modules that can "signal" for control of the bus).

Control Bus signals (memory access)

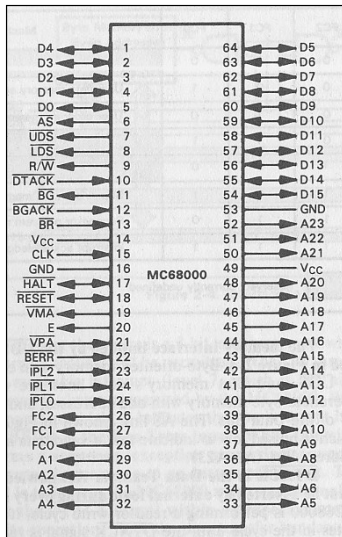
- ✓ Address Strobe: valid address on the Address Bus (AS).
- ✓ Read/Write: $R/\overline{W} = 1$, reading from memory, $R/\overline{W} = 0$, writing to memory.
- ✓ Upper/Lower Data Strobes: (\overline{LDS} , \overline{UDS}) encodes state of LSB of Address Bus, allowing specification of byte-mode transfers to/from memory.
- ✓ Chip Select – (CS) indicates even or odd-byte access from memory (organized into 2 banks of 2^{24} words with each bank storing one byte of the two-byte word).
- ✓ Data Transfer Acknowledge: (DTACK) indicates data cycle completion. It is generated through the Address decode circuitry, and can constitute multiple "wait states"



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M68K Architecture – Pinout Inventory

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Pin Name	Description	Type
D0-D15	Data Bus	Bidirectional, Tristate
A1-A23	Address Bus	Output, Tristate
AS	Address Strobe	Output, Tristate
R/ \overline{W}	Read/Write Control	Output, Tristate
\overline{UDS} , \overline{LDS}	Upper, Lower Data Strobes	Output, Tristate
DTACK	Data Transfer Acknowledge	Input
FC0, FC1, FC2	Function Code (status) Outputs	Output, Tristate
IPL0, IPL1, IPL2	Interrupt Requests	Input
BERR	Bus Error	Input
HALT	Halt Processor Operation	Input/Output
RESET	Reset Processor or Reset External Devices	Input/Output
CLK	System Clock	Input
BR	Bus Request	Input
BG	Bus Grant	Output
BGACK	Bus Grant Acknowledge	Input
E	Enable (Clock) Output	Output
VMA	Valid Memory Address	Output, Tristate
VPA	Valid Peripheral Address	Input
Vcc, GND	Power (+5 V) and Ground	

- NOTE: Most of the control bus signals are either "active low" (i.e., they are True when set low) or they are toggled signals (i.e., both values are significant for control functions).



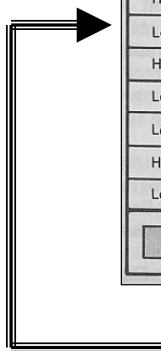
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M68K Architecture – Bus Control Signals

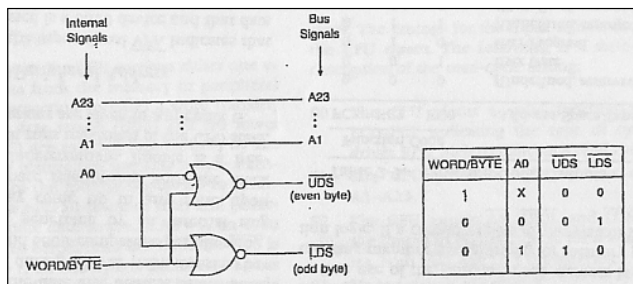
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\overline{UDS}	\overline{LDS}	R/W	D8-D15	D0-D7	Operation
High	High				
Low	Low	High	Data bits 8-15	Data bits 0-7	Word Read
High	Low	High		Data bits 0-7	Byte Read
Low	High	High	Data bits 8-15		Byte Read
Low	Low	Low	Data bits 8-15	Data bits 0-7	Word Write
High	Low	Low	Data bits 0-7	Data bits 0-7	Byte Write
Low	High	Low	Data bits 8-15	Data bits 8-15	Byte Write

No valid data output or input



- Note the internal logic for generating the \overline{UDS} and \overline{LDS} signals. The scenario of both going high without a valid Read/Write signal.

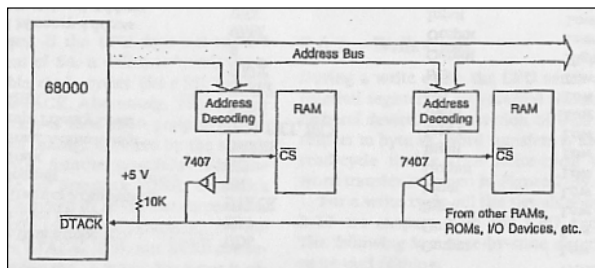
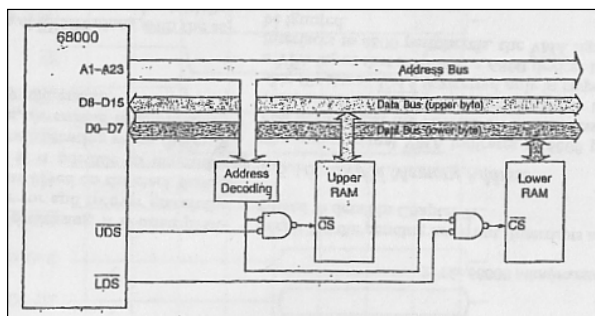


Source: MacKenzie © 1995 Prentice Hall Publishers



M68K Architecture – Memory Access Control

Source: MacKenzie © 1995 Prentice Hall Publishers



- Access Cycle setup:
 - Address is placed on the Address Bus (pins A1-A23).
 - Pin A0 set/cleared to indicate byte-mode transfer.
 - Read/Write flag set to indicate type of memory access.
 - Data Strobes set, based on A0 value, and whether byte-mode.
 - Chip Select derived from address decoding logic (as we discussed in previous lecture) and data strobe.
- Access Completion
 - Data transfer Acknowledge set low on completion of operation (CPU only gets confirmation on read from memory into register).
 - On DTACK (low), the CPU sets AS to high, clears Address lines, and either latches the data (on read) or clears data (on write).

