



CSCE 611

Digital Systems Design I

2005/4/20

Week 13-B Supplemental Notes

Exam #2 Study Example – Traffic Light Controller

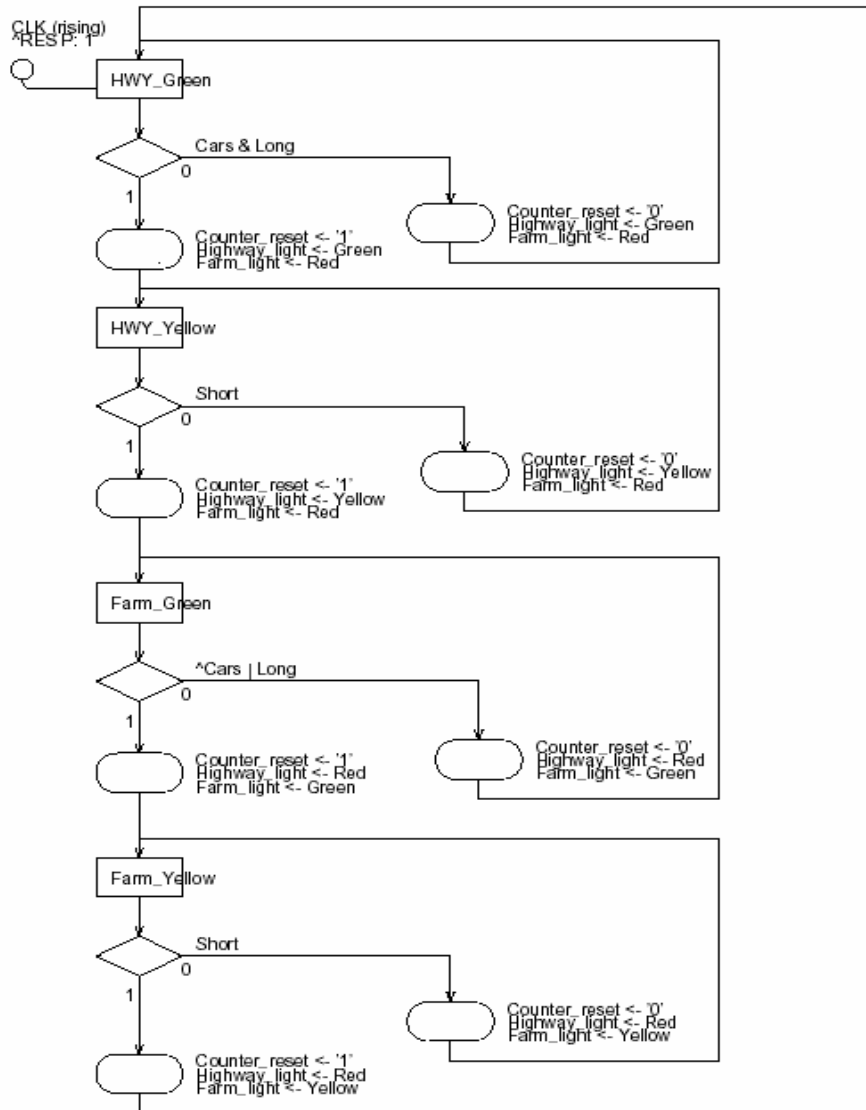
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Example source: Wolf © 2004 Prentice-Hall Publishers, Inc.

Week 13 – Problem Example

- Wolf, Chapter 5, Sequential Design, pp. 331-337.
 - Traffic Light Controller example.
 - Wolf provides state diagram for Sequencer thread, and talks about the Counter thread (from the Verilog code)
- We model as 2 communicating ASM threads, and discuss the following mappings:
 - ASM to register-level data path diagram, indicating the “control points” for selecting specific actions by the state machine.
 - ASM to next state and output decoding equations for the state machine in the control path (we only look at the Sequencer).
 - ASM model to realization of the state machine, including how we generate both the combinational and register logic using LUT and register structures found in Xilinx FPGA CLBs.
 - ASM register and macro-function assignment statements, and the data path computing logic and intermediate storage registers—using truth tables.
 - CLB structure for Xilinx Spartan 2E®

Sequencer – Next State Equations



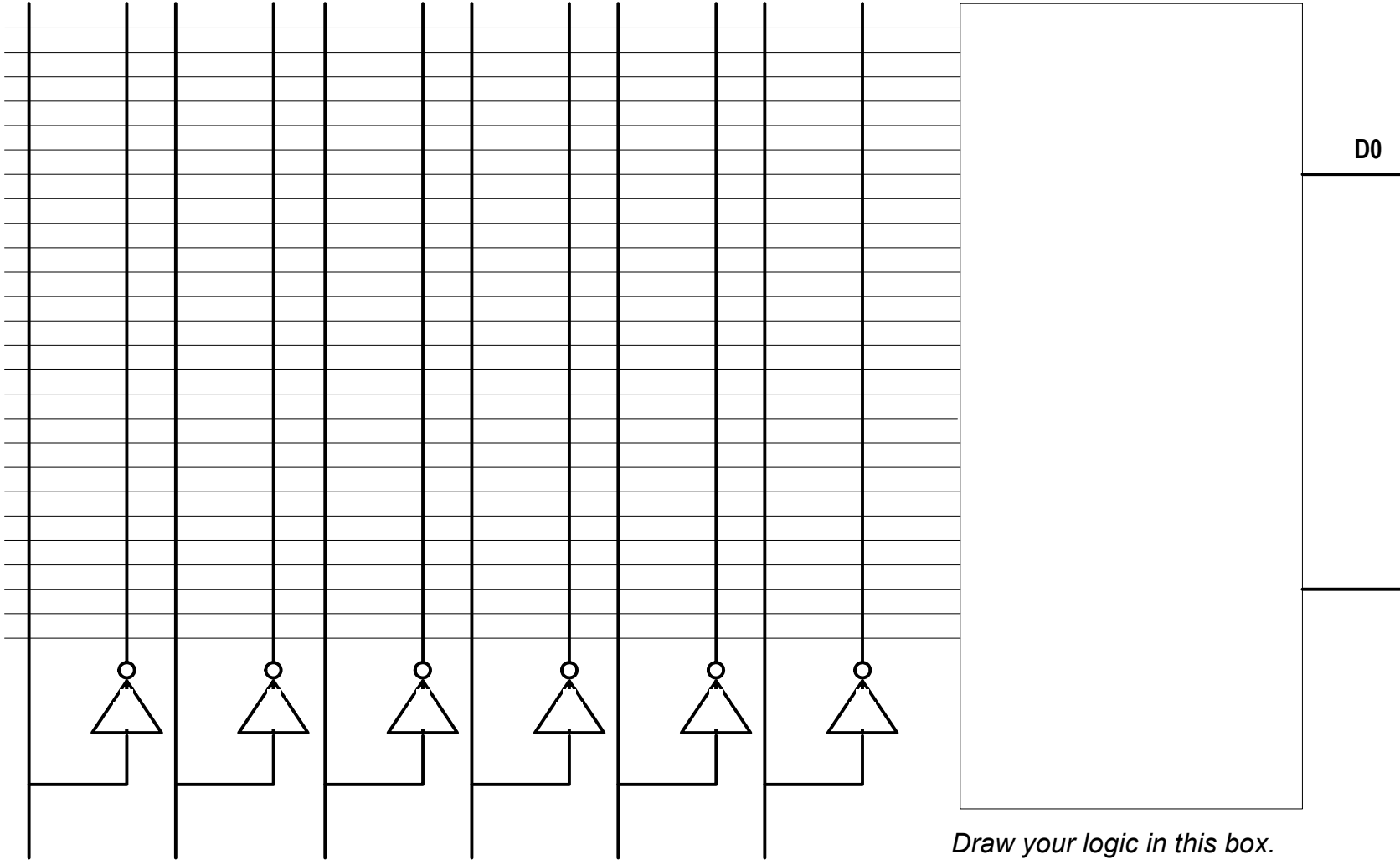
Write your **next state** equations here:

Sequencer – Next State Truth Table

Cars	Short	Long	Q1	Q0	Next State Decoding Logic					D1	D0	
					D1	D0	Cars	Short	Long			Q1
0	0	0	0	0			1	0	0	0		
0	0	0	0	1			1	0	0	0		1
0	0	0	1	0			1	0	0	1		0
0	0	0	1	1			1	0	0	1		1
0	0	1	0	0			1	0	1	0		0
0	0	1	0	1			1	0	1	0		1
0	0	1	1	0			1	0	1	1		0
0	0	1	1	1			1	0	1	1		1
0	1	0	0	0			1	1	0	0		0
0	1	0	0	1			1	1	0	0		1
0	1	0	1	0			1	1	0	1		0
0	1	0	1	1			1	1	0	1		1
0	1	1	0	0			1	1	1	0		0
0	1	1	0	1			1	1	1	0		1
0	1	1	1	0			1	1	1	1		0
0	1	1	1	1			1	1	1	1		1

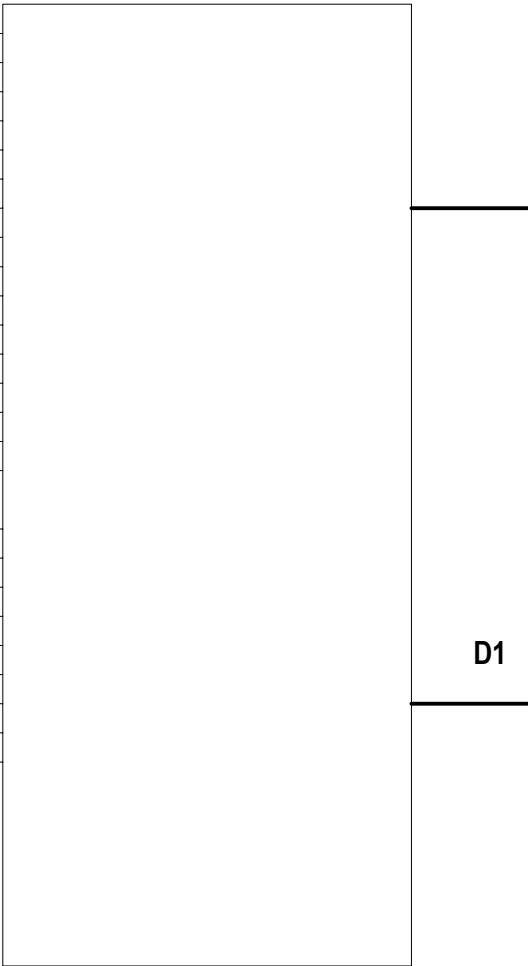
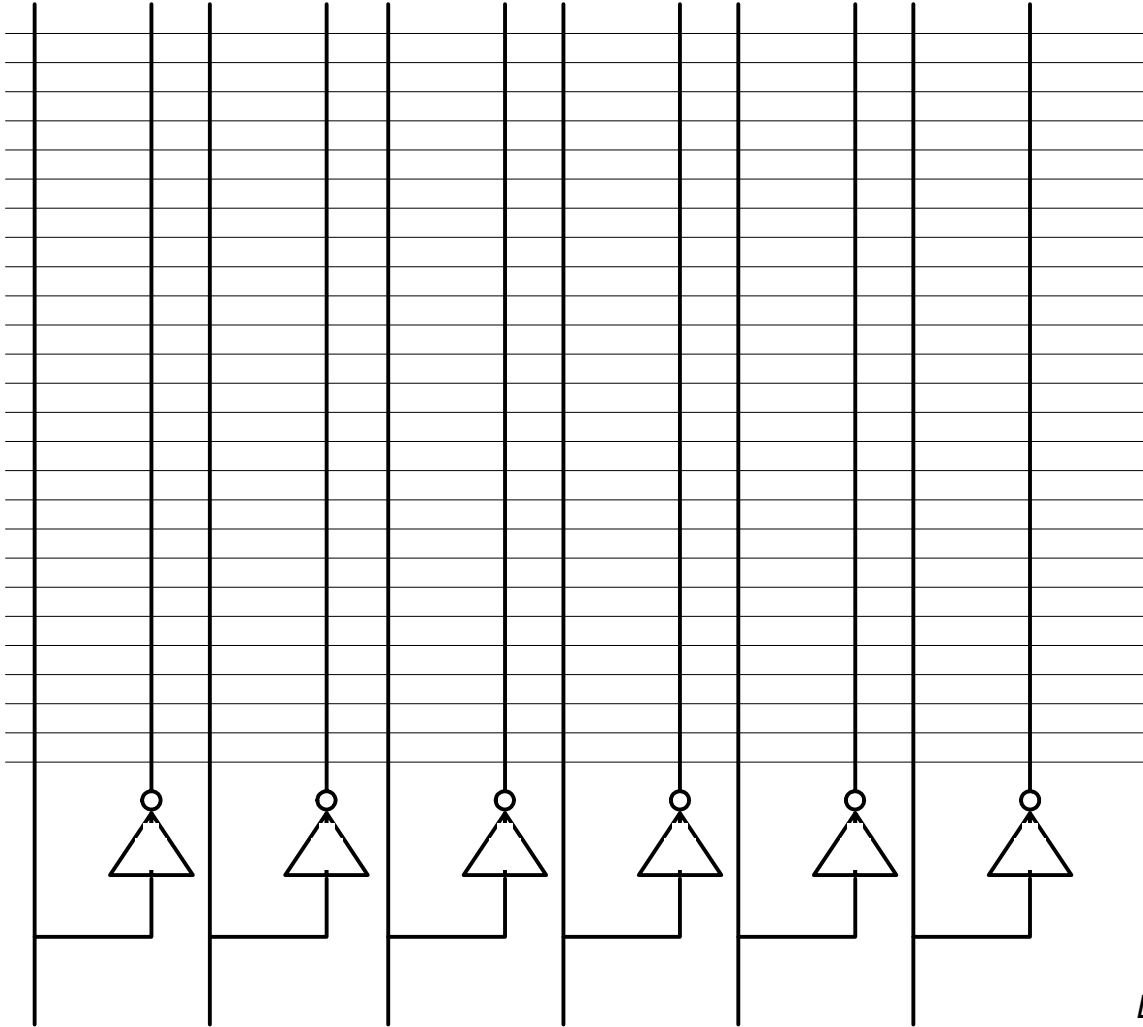
• We need the truth tables for the next state and output decoding logic feeding the state machine.

Sequencer – Next State Look-Up Table-D0



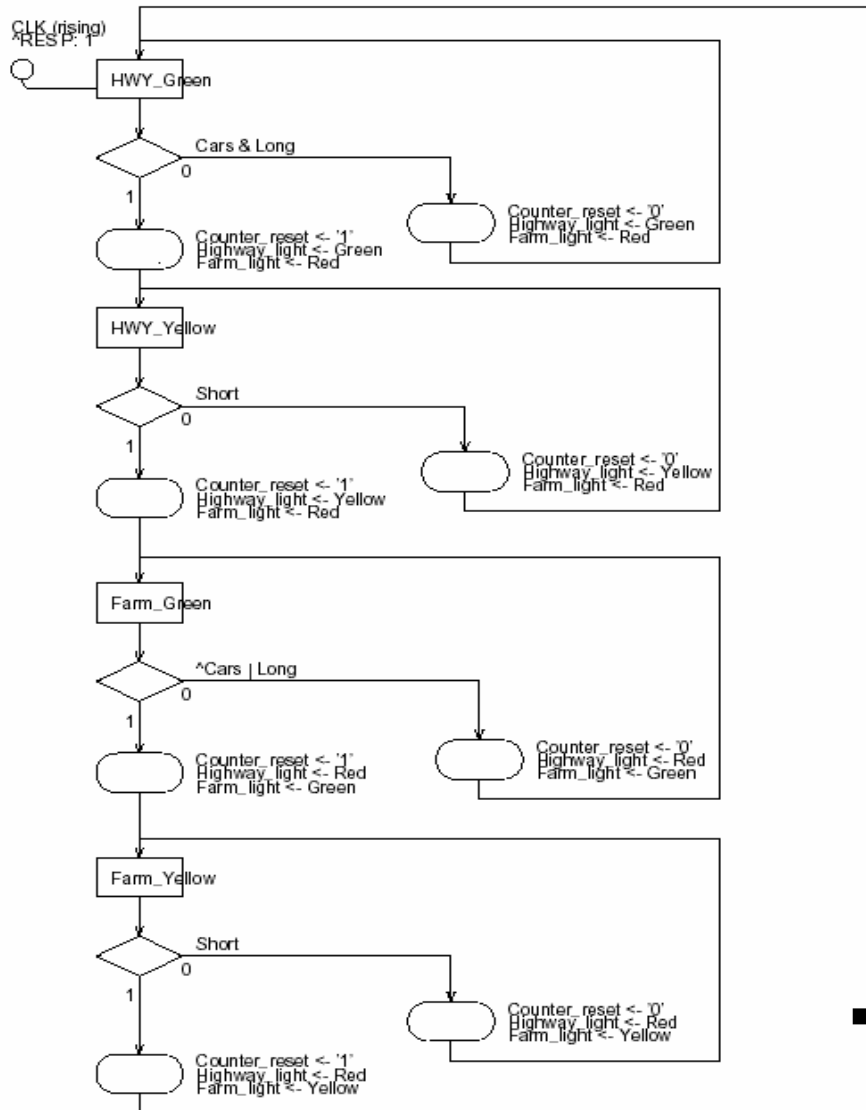
*Draw your logic in this box.
Connect and label your signals.*

Sequencer – Next State Look-Up Table-D1



*Draw your logic in this box.
Connect and label your signals.*

Sequencer – Output Equations



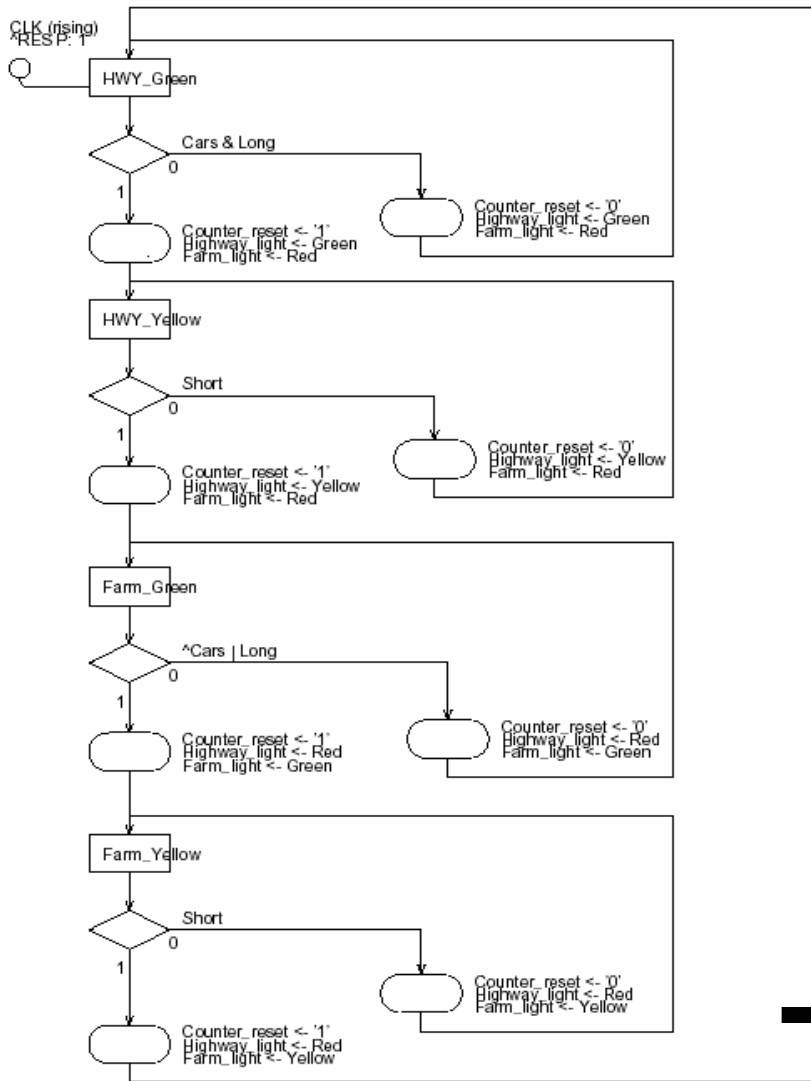
Write your **output** equations here:

Sequencer – Output Truth Tables

					Output Decoding Logic																				
Cars	Short	Long	Q1	Q0	CR1	CR0	HG	HY	HR	FG	FY	FR	Cars	Short	Long	Q1	Q0	CR1	CR0	HG	HY	HR	FG	FY	FR
0	0	0	0	0									1	0	0	0	0								
0	0	0	0	1									1	0	0	0	1								
0	0	0	1	0									1	0	0	1	0								
0	0	0	1	1									1	0	0	1	1								
0	0	1	0	0									1	0	1	0	0								
0	0	1	0	1									1	0	1	0	1								
0	0	1	1	0									1	0	1	1	0								
0	0	1	1	1									1	0	1	1	1								
0	1	0	0	0									1	1	0	0	0								
0	1	0	0	1									1	1	0	0	1								
0	1	0	1	0									1	1	0	1	0								
0	1	0	1	1									1	1	0	1	1								
0	1	1	0	0									1	1	1	0	0								
0	1	1	0	1									1	1	1	0	1								
0	1	1	1	0									1	1	1	1	0								
0	1	1	1	1									1	1	1	1	1								

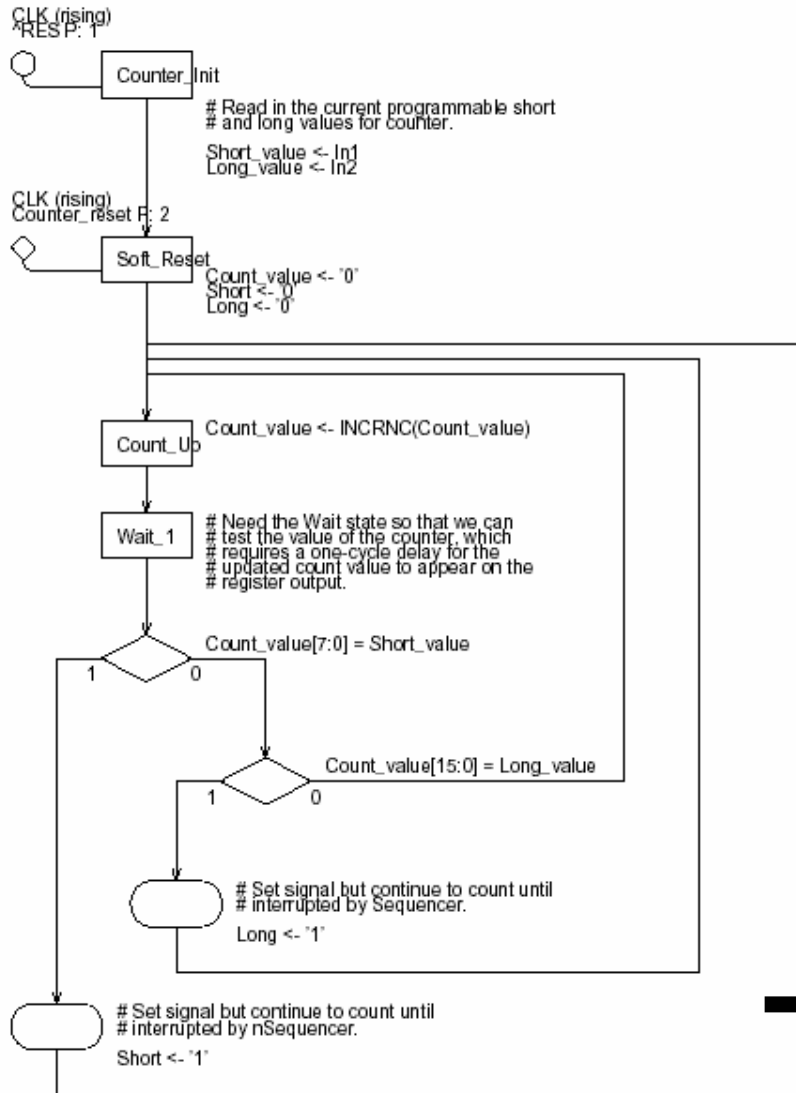
- We need the truth tables for the next state and output decoding logic feeding the state machine.

Traffic Light Sequencer – Data Path



Draw your data path diagram here:

Counter – Next State Equations



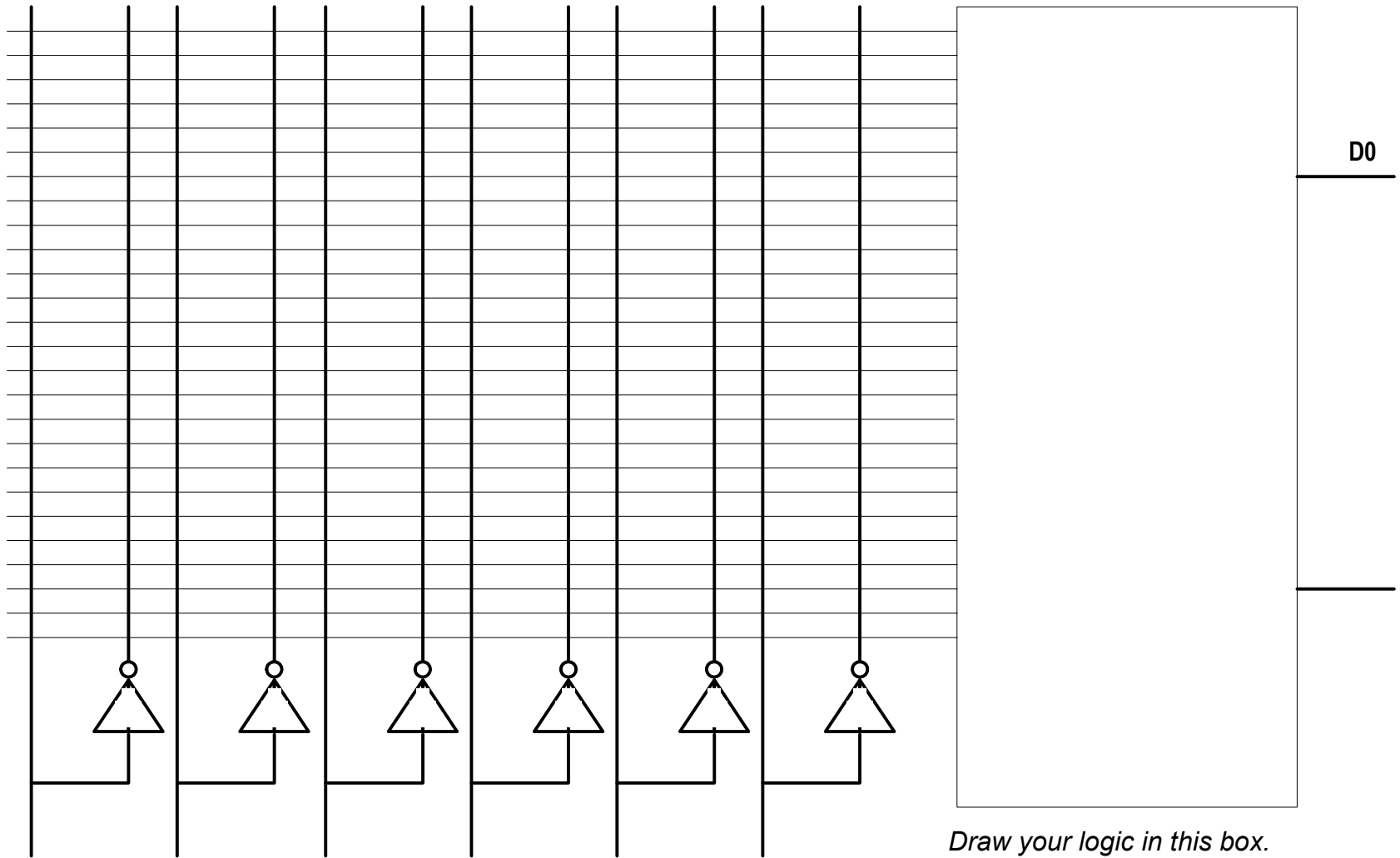
Write your **next state** equations here:

Counter – Next State Truth Table

Next State Decoding Logic

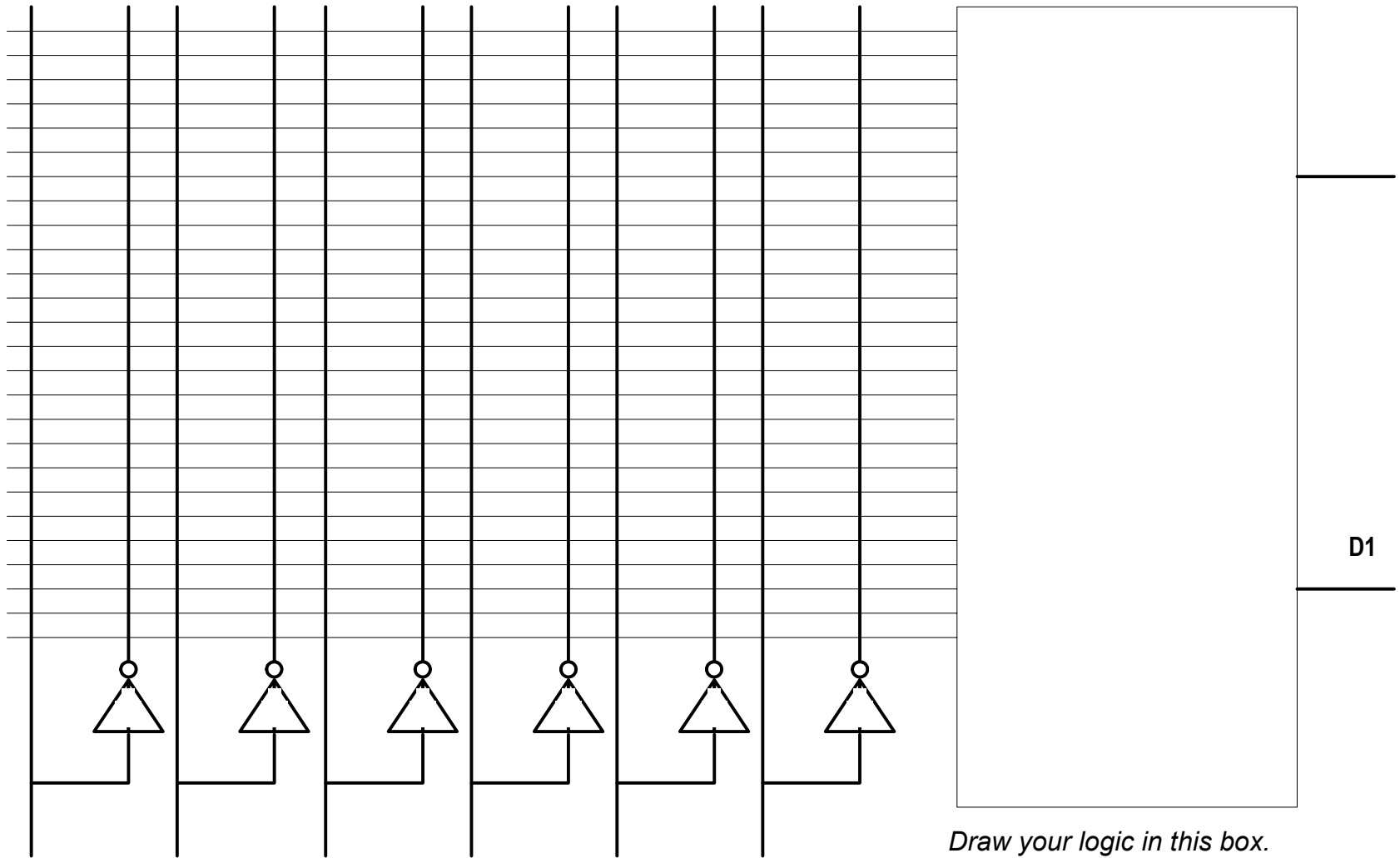
- We need the truth tables for the next state and output decoding logic feeding the state machine.

Counter – Next State Look-Up Table-D0



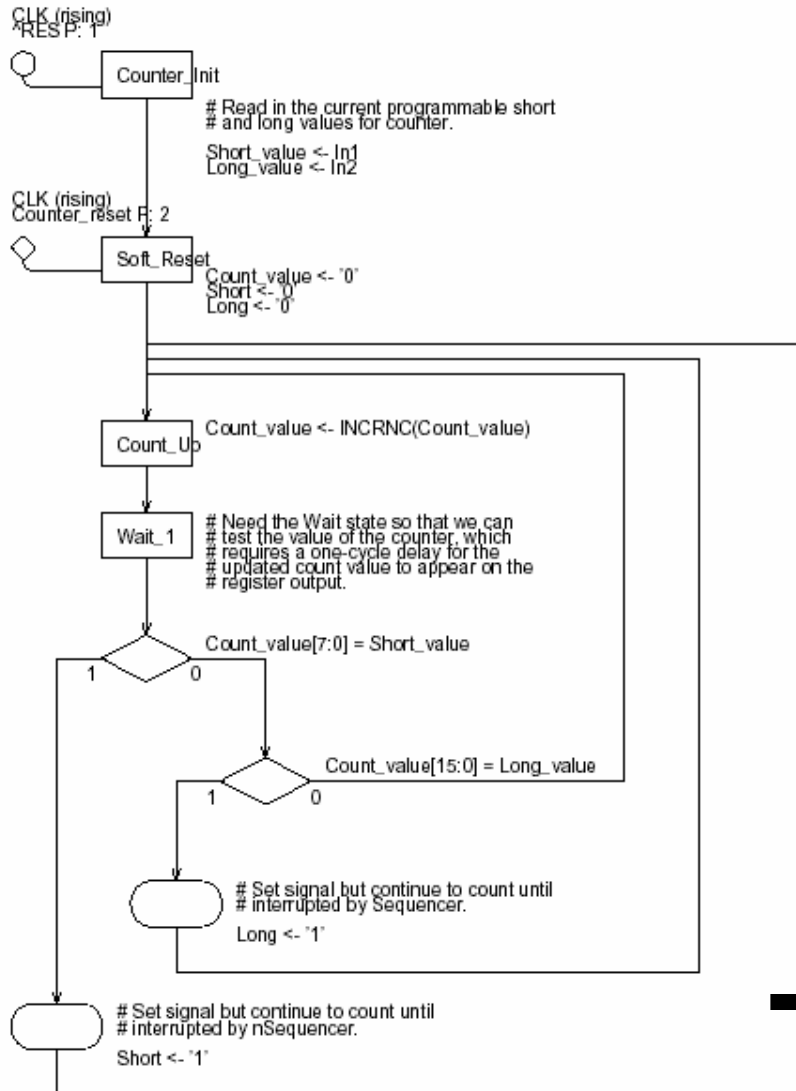
*Draw your logic in this box.
Connect and label your signals.*

Counter – Next State Look-Up Table-D1



*Draw your logic in this box.
Connect and label your signals.*

Traffic Light Counter – Output Equations



Write your **output** equations here:

Counter – Output Truth Tables

Output Decoding Logic

- We need the truth tables for the next state and output decoding logic feeding the state machine.

Traffic Light Counter – Data Path

