

Introduction

The Spartan™-II E 1.8V Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The seven-member family offers densities ranging from 50,000 to 600,000 system gates, as shown in [Table 1](#). System performance is supported beyond 200 MHz.

Spartan-II E devices deliver more gates, I/Os, and features per dollar than other FPGAs by combining advanced process technology with a streamlined architecture based on the proven Virtex™-E platform. Features include block RAM (to 288K bits), distributed RAM (to 221,184 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-II E family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
 - Densities as high as 15,552 logic cells with up to 600,000 system gates
 - Streamlined features based on Virtex-E architecture
 - Unlimited in-system reprogrammability
 - Very low cost
 - Advanced 0.15 micron technology

- System level features
 - SelectRAM+™ hierarchical memory:
 - 16 bits/LUT distributed RAM
 - Configurable 4K-bit true dual-port block RAM
 - Fast interfaces to external RAM
 - Fully 3.3V PCI compliant to 64 bits at 66 MHz and CardBus compliant
 - Low-power segmented routing architecture
 - Dedicated carry logic for high-speed arithmetic
 - Efficient multiplier support
 - Cascade chain for wide-input functions
 - Abundant registers/latches with enable, set, reset
 - Four dedicated DLLs for advanced clock control
 - Eliminate clock distribution delay
 - Multiply, divide, or phase shift
 - Four primary low-skew global clock distribution nets
 - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
 - Pb-free package options
 - Low-cost packages available in all densities
 - Family footprint compatibility in common packages
 - 19 high-performance interface standards
 - LVTTTL, LVCMOS, HSTL, SSTL, AGP, CTT, GTL
 - LVDS and LVPECL differential I/O
 - Up to 205 differential I/O pairs that can be input, output, or bidirectional
 - Hot swap I/O (CompactPCI friendly)
- Fully supported by powerful Xilinx ISE development system
 - Fully automatic mapping, placement, and routing
 - Integrated with design entry and verification tools
 - Extensive IP library including DSP functions and soft processors

Table 1: Spartan-II E FPGA Family Members

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O ⁽¹⁾	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	265	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

Notes:

1. User I/O counts include the four global clock/user input pins. See details in [Table 2, page 3](#)

General Overview

The Spartan-IIE family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. The XC2S400E has four columns and the XC2S600E has six columns of block RAM. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see [Figure 1](#)).

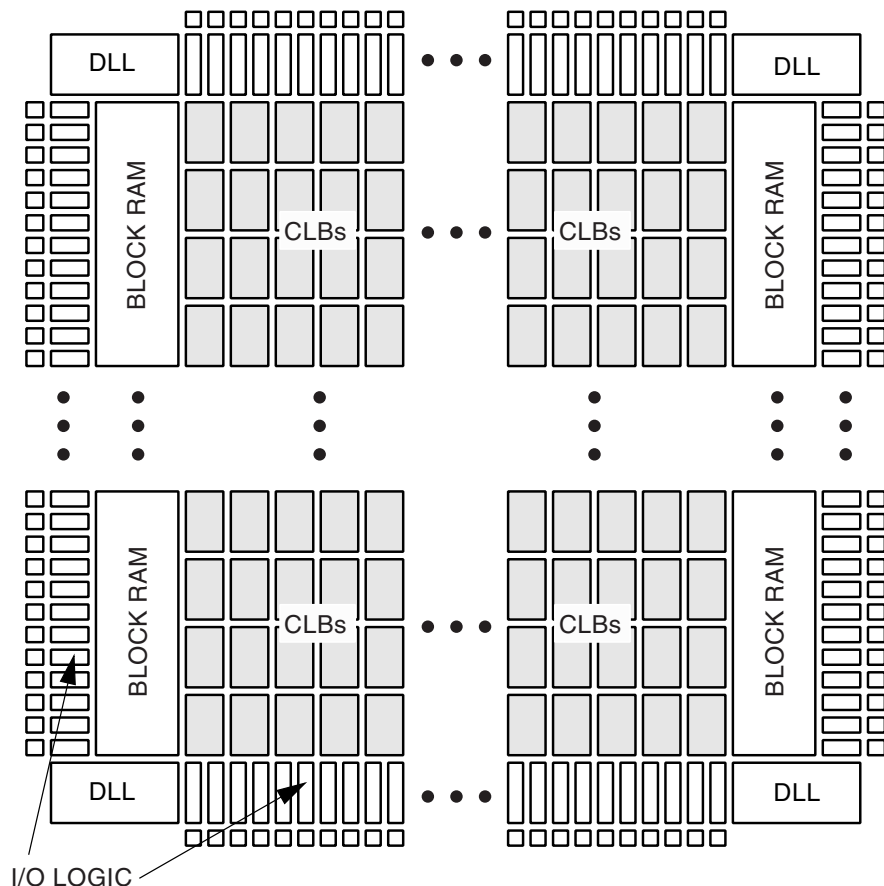
Spartan-IIE FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes. Xilinx offers multiple types of low-cost configuration solutions including the Platform Flash in-system programmable configuration PROMs.

Spartan-IIE FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-IIE FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-IIE FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-IIE devices provide system clock rates beyond 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-IIE FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

Spartan-IIE Family Compared to Spartan-II Family

- Higher density and more I/O
- Higher performance
- Unique pinouts in cost-effective packages
- Differential signaling
 - LVDS, Bus LVDS, LVPECL
- $V_{CCINT} = 1.8V$
 - Lower power
 - 5V tolerance with external resistor
 - 3V tolerance directly
- PCI, LVTTTL, and LVCMOS2 input buffers powered by V_{CCO} instead of V_{CCINT}
- Unique larger bitstream



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Figure 1: Basic Spartan-IIE Family FPGA Block Diagram

Spartan-IIE Product Availability

Table 2 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination.

Table 2: Spartan-IIE User I/O Chart

Device	Maximum User I/O	Available User I/O According to Package Type				
		TQ144 TQG144	PQ208 PQG208	FT256 FTG256	FG456 FGG456	FG676 FGG676
XC2S50E	182	102	146	182	-	-
XC2S100E	202	102	146	182	202	-
XC2S150E	265	-	146	182	265	-
XC2S200E	289	-	146	182	289	-
XC2S300E	329	-	146	182	329	-
XC2S400E	410	-	-	182	329	410
XC2S600E	514	-	-	-	329	514

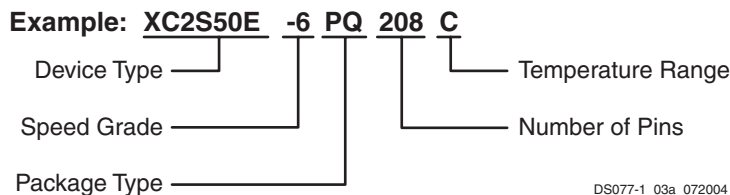
Notes:

1. User I/O counts include the four global clock/user input pins.

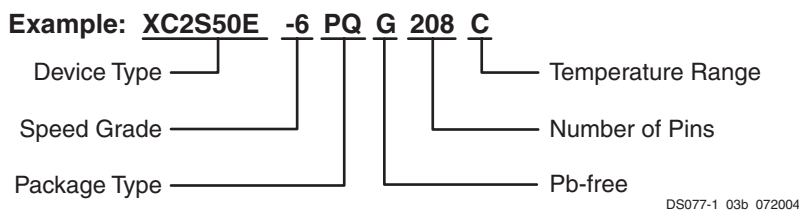
Ordering Information

Spartan-II E devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

Standard Packaging



Pb-Free Packaging



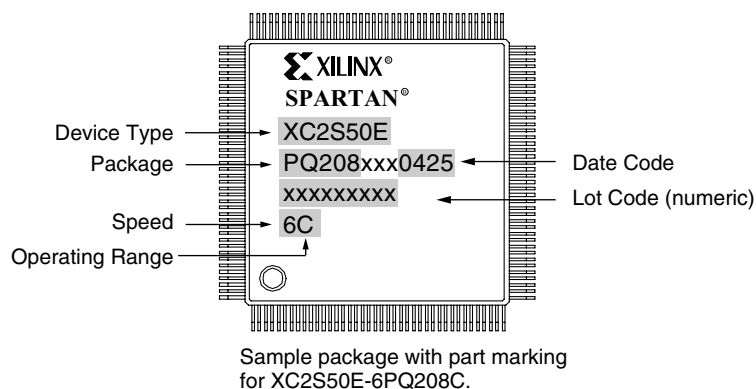
Device Ordering Options

Device	Speed Grade		Package Type / Number of Pins		Temperature Range (T_J) ⁽²⁾	
	XC2S50E	-6	Standard Performance	TQ(G)144	144-pin Plastic Thin QFP	C = Commercial
XC2S100E	-7	Higher Performance ⁽¹⁾	PQ(G)208	208-pin Plastic QFP	I = Industrial	-40°C to +100°C
XC2S150E			FT(G)256	256-ball Fine Pitch BGA		
XC2S200E			FG(G)456	456-ball Fine Pitch BGA		
XC2S300E			FG(G)676	676-ball Fine Pitch BGA		
XC2S400E						
XC2S600E						

Notes:

- The -7 speed grade is exclusively available in the Commercial temperature range.
- See www.xilinx.com for information on automotive temperature range devices.

Device Part Marking



The Spartan-IIe Family Data Sheet

DS077-1, *Spartan-IIe 1.8V FPGA Family: Introduction and Ordering Information* (Module 1)

DS077-2, *Spartan-IIe 1.8V FPGA Family: [Functional Description](#)* (Module 2)

DS077-3, *Spartan-IIe 1.8V FPGA Family: [DC and Switching Characteristics](#)* (Module 3)

DS077-4, *Spartan-IIe 1.8V FPGA Family: [Pinout Tables](#)* (Module 4)

Revision History

Date	Version No.	Description
06/27/02	1.1	Updated -7 availability.
11/18/02	2.0	Added XC2S400E and XC2S600E. Corrected XC2S150E max I/O count and XC2S50E differential I/O count and updated availability.
07/09/03	2.1	Noted hot-swap capability. Updated Table 2 to show that all products are available. Clarified device part marking.
07/28/04	2.2	Added information on Pb-free packaging options.