

## Working in the Mentor Environment – Part 2

### 3. IC Station Tutorial

This document contains a step-by-step tutorial for generating the layout of an inverter in the Mentor Graphics application IC Station. It covers the following steps: (1) opening IC station and creating a cell, (2) generating a circuit layout, and (3) checking the design for errors (DRC and LVS checking).

#### 3.1 General Information

To this point, we have completed schematic entry in the Design Architect (DA) tools. We also created the design viewpoint for the inverter cell completed in DA. You should be familiar with the mask layers and design rules discussed in class; the rules for Mentor are covered in the DRC Rules section at the end of this document.

Note, throughout this tutorial, we use both  $L$  and  $\square$  to represent the minimum feature size  $\lambda$ .

#### Preparing the design for use in IC station:

The viewpoint you created using DA is needed for layout and verification. You only have to do this once per design. Even if you make changes to your design you don't have to do this again. If you decide to change the underlying technology library, however, you must rerun the script with the appropriate technology parameter.

#### 3.2 Opening IC

##### 3.2.1 Opening IC station:

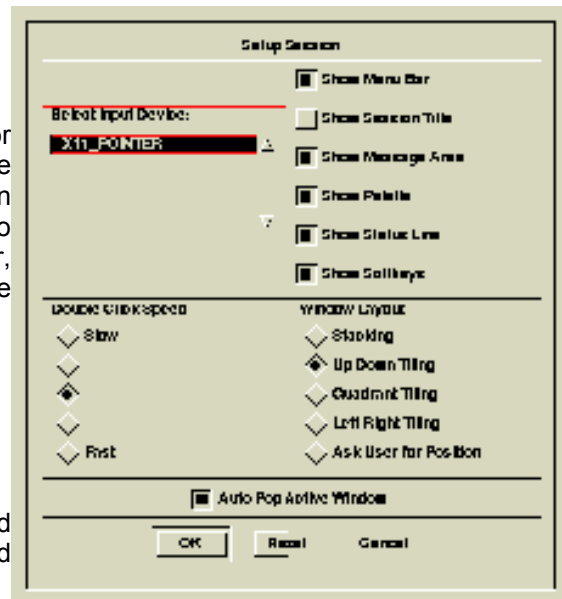
Make sure you are in your 613 working directory and you have run the script. Then, at the command prompt, enter the following:

```
% setenv MGC_WD $HOME/csce613  
  
% source /usr/local/etc/mgc-ADK.csh  
  
% ic &
```

##### 3.2.2 Setting Up IC Station:

Maximize the IC Station window so you have lots of room to work on your layout, and setup your environment by selecting the following from the main menu:

MGC > Setup > Session



and selecting *Up Down Tiling* from the Window Layout portion of the dialog box. Leave everything else as default and click 'OK'.

### 3.2.3 Creating your Cell

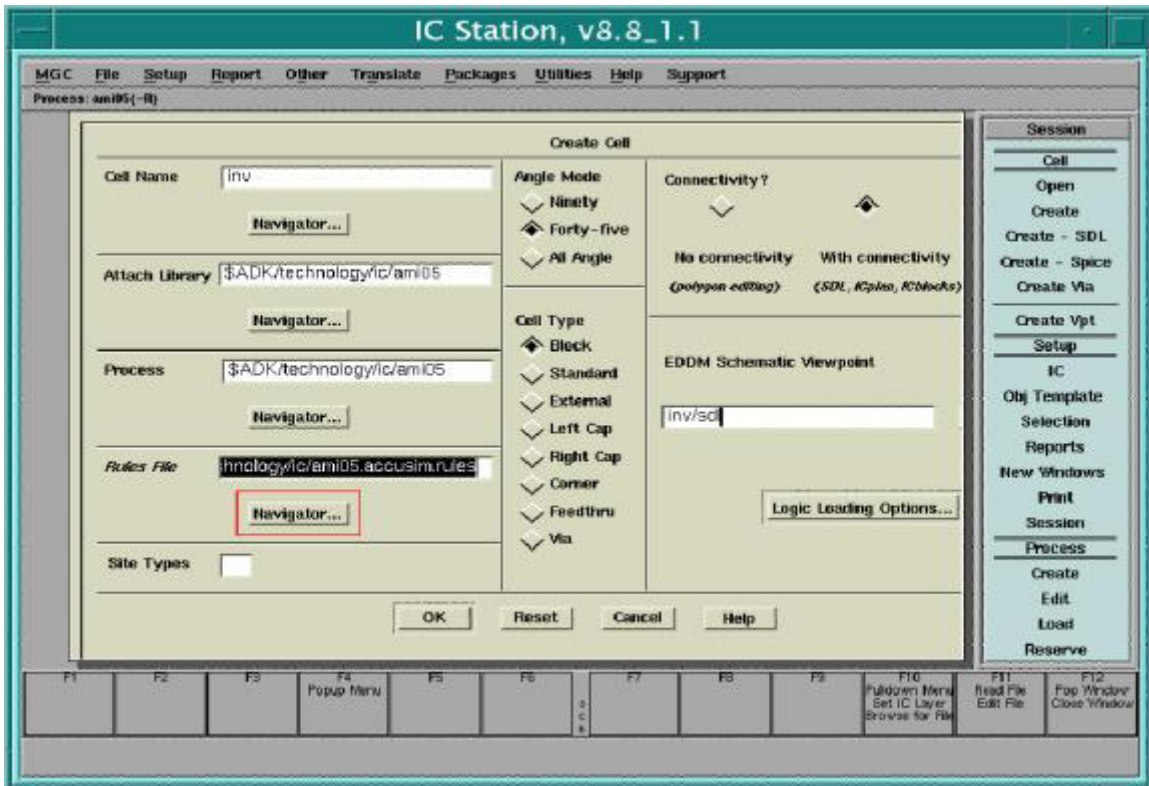
From the main *Session Palette* on the right, select

Create (under heading of *Cell*)

or alternatively, using the main menu, select

File > Cell > Create

The figure below shows the dialog box window that should pop up. In the *Cell Name* space, enter the name of the cell as *inv*.



Click on the Navigator button under *Attach Library* then click on the 4-direction arrows and enter the directory (if you are going to use primitive nMOS and pMOS devices to lay out inverters and other logic gates.

```
/usr/local/mgc_tree/ADK/technology/ic/
```

then click 'OK' to view all available libraries. Select 'ami05' (choose the icon with the 'L' symbol, not the folder symbol) and click 'OK'.

Follow the same procedure for *Process* and select 'ami05' (choose the file with the 'P' icon, not the folder icon).



### View > Zoom > To Grid

Your layout window will now show the smallest grid point to which you can align your layer polygons. The spacing between two immediate dots in the grid is  $0.5L$  or  $0.5\lambda$  (i.e., 2 grid points equals  $1\lambda$ ). Use this grid to help determine the size of each polygon you draw. Also notice near the center of this window you will see a large white + symbol. This represents the origin of the cell and is the 0,0 point for the position cursor which is constantly updated just above your layout window and below the main menu bar. Typically we want to set the origin of each cell to the lower left corner. More discussion on cell origin is provided later in the tutorial.



### 3.3.3 Adding Shapes

From the main *IC Palette*, select

Easy Edit > Shape

This will open a dialog box at the bottom of the screen titled 'ADD SH'. Click on the Options tab to view and select the layers you will need to draw your transistors. See DRC Rules at the end of this tutorial for a list of the layers you will need.

You can either select a layer by clicking on it, or you can type the name of the layer in the *Or Type In* box. Click the 'Keep Option Settings' button if you want this layer to be the default layer (i.e., it will automatically be selected each time you use the Add Shape command). Use the scroll bar to move down to layer 43, *ACTIVE*. Select this layer and click OK.

Scroll down the list to find the layer you want. Start by next choosing the active layer. Click on *Active* and then click OK. The mouse pointer changes to + format. In the layout cell window, click and drag on the canvas to form a rectangle that is  $15L$  (width) x  $5L$  (height). At this point the polygon is selected and will appear as an unfilled rectangle. Press F2 to unselect the object and it will fill with the pattern for that layer.

Note: the function keys, in combination with shift/control/alt, provide you with many commands that you will use often. These are shown at the bottom of the IC window. Practice using the functions, for Select, Unselect, Move, and Copy operations. When you are done, save only one *ACTIVE* rectangle and delete all others.

#### 3.3.4. Adding more layers:

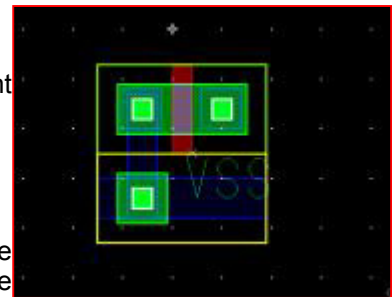
Next, add a *POLY* layer. Draw a rectangle 2L (width) x 9L (height) ( $W/L=5/2$ ) cutting midway through the *ACTIVE* layer such that the top and bottom of *POLY* rectangle are 2L above and below the *ACTIVE* layer.

Continue selecting new layers and adding to form the transistor. Cover the *ACTIVE* layer with a *N\_PLUS\_SELECT* (which we'll call *N-SELECT*) layer to begin forming an nMOS transistor (notice we do not have a N-Well layer, consistent with an nMOS device). The *N-SELECT* layer should overlap the *ACTIVE* by 2L on all sides (constrained by the design rules). The region where *POLY* overlaps the *ACTIVE* layer with *N-SELECT* forms the n-type MOS Gate. To form a p-gate we would need an N-Well and would replace N-Select with P-Select.

Note there are many editing functions that allow you to cut, notch, stretch, etc. any polygon you draw. You will need to become familiar with many of these functions. More information on these is provided in the section labeled Editing Cell Layout. If you practice these functions, make sure you have only the layers specified above when you return to this part of the tutorial.

To form a *substrate tap*, you will need a combination of the layers *ACTIVE* and *P-SELECT*. Add a tap now. Later we will want to form an *n-well tap*, which will need a combination of *ACTIVE* and *N-SELECT* inside an *N-WELL* layer. These taps are also called *pdiff* and *ndiff*.

For this tutorial, we will build a single nMOS transistor and its associated substrate tap. It should look like the figure to the right, except without contacts and metal, both of which will be added later. Make your layout looks like the figure before moving to the next steps.



At this point, let's save the cell so we don't lose any work in the event of a computer crash. So, select the following:

File > Cell > Save Cell > Current Context

Before we can continue, we need to reserve our cell. Every time we save the cell, it will no longer be reserved for editing. So, because you want to modify your cell, select the following:

File > Cell > Reserve > Current context.

#### 3.3.5. Checking the layout:

Once you have the basic layers for your transistor, you should check to make sure you have not violated any design rules. You will want to do this frequently during the design process, as you layer on functionality, so that you can correct errors as they occur rather than waiting until you are done when you might have many more errors to correct. Look at the section on Design Rules Checker to see how these are used.

Note: This first time through the DRC check, you will get one or more 'bad\_contact' (or similar) errors. Ignore these for now, as we'll will fix them in the next step.

### 3.3.6. Making contacts:

Now we need to create electrical connections from the active regions to upper-level metal layers which we will do using *contact* layers. We will be using two different contact layers, one for contact to the active region, *CONTACT\_TO\_ACTIVE*, and one for contact between metal1 and poly, *CONTACT\_TO\_POLY*. To simplify, we will use the terms *ACONT* and *PCONT*, respectively, as given in the DRC section.

Consider first the nMOS transistor. Since this is an n-well CMOS process, the nMOS transistors must be formed in the p-substrate with an associated substrate contact called a “tap”. The substrate will be connected to the ground or VSS of the circuit. The source of the nMOS transistor will also be connected to ground, and the drain of the transistor will (eventually) be connected to the output node.

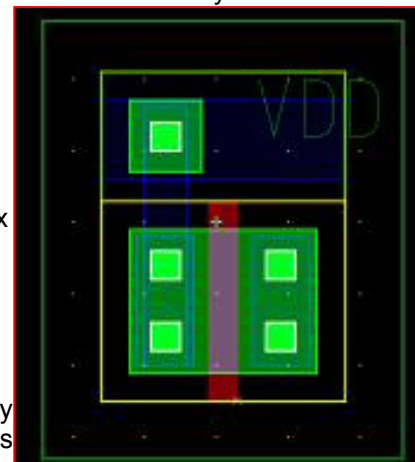
Using the *ACONT* (*CONTACT\_TO\_ACTIVE*) layer, add contacts to the source and drain following the *Adding Shapes* step above. Next add a contact to the tap active layer. Then, add a *METAL1* layer across the bottom of your transistor, covering the tap contact and stretching across the full width (left-to-right) of the *P-SELECT* layer. This will form the ground power supply rail in your design (discussed more in the note below). You should make the *METAL1* ground rail as wide as the tap active layer (5L). Although this is larger than the minimum size of metal1, we want the ground (and VDD) rails to be able to handle more current and therefore be wider than minimum size.

Finally, you need to connect the source of the transistor to the ground rail using *METAL1*. You can either add a new polygon to connect the source contact (left side of the transistor) to the tap contact, or you can try the *notch* command to modify the metal1 power rail polygon. Either way, make sure your source and substrate tap are connected.

When you are done, your cell should look very similar to the figure below. Save your cell and then reserve it for edit before continuing.

### 3.3.7. Do it All Again

Repeat the processes above to form a pMOS transistor with a tap to the n-well. Your pMOS transistor should have  $W/L = 10L/2L$  to match your schematic (you will need to draw the active layer  $15L \times 10L$ ). You will, of course, also have to add the *N-WELL* layer which should surround your transistor and tap active layers according to the design rules. Once you have added all of the shapes, your pMOS should look like the figure to the right.

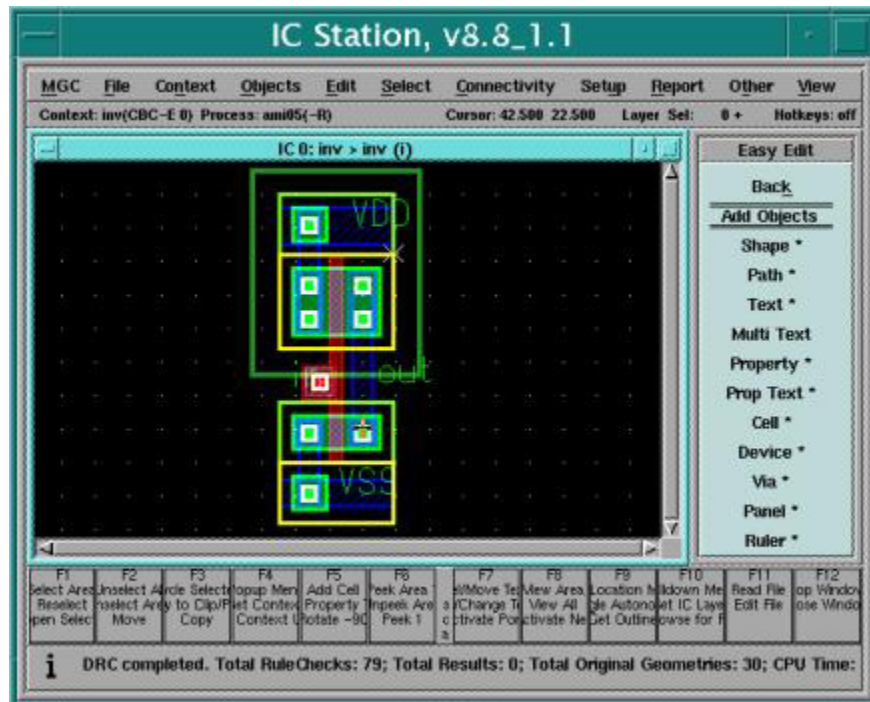


Note about cell *pitch*. In large-scale VLSI design (i.e., with many transistors/gates/cells), it is important to make the cell layouts have uniform height so that they will match when placed side-by-side. Typically, we will design each gate with a VDD rail at the top and a Ground rail at the bottom. If we place two cells together, we want these power rails to match-up. This will make more sense when we start putting several gates together to form a logic function. We define *pitch* as *the distance from top to bottom of our layout cell*, measured from the top of the VDD rail to the bottom of the Ground rail. For our purposes, we will use a cell pitch of  $50\lambda$ . Some larger cells might not match this size, but all the basic logic gates should have a layout height of  $50\lambda$ .

### 3.3.8 Final Layout Steps

Finally, we obtain the layout of the inverter by stacking the two transistors and connecting them as required. Connect the drains using *METAL1* to form the output. Join the *POLY* of the two gates to form the input by adding another polygon or modifying one of the existing poly lines.

Since we often want to connect to the input gates from metal1, you should add a metal1 contact to poly on your input. Notch your *POLY* input near the middle of the cell to be at least 5Lx5L, add *METAL1* on top of this, then add *PCONT* (*CONTACT\_TO\_POLY*) in the center of these shapes. The final layout should be very similar to that shown below.



Once you think you have the layout complete, you should run the check for DRC errors and fix them before continuing. Consult the Design Rules Checker section first, then come back here and continue.

### 3.3.9. Adding the ports

In order for the software tools to match your layout to a schematic, we need to assign a few port values to our input and output nodes. The first step is to make sure you have deselected everything on the canvas by pressing F2. Then, select the layer to which a port connection is to be made. For this example, we want to make the *metal1* layer that connects the two drains into an output port, and the *metal1* layer that is connected to the gate poly to be an input port. Do these one-at-a-time, and be sure to unselect one by pressing F2 before selecting the other.

With the desired layer selected, so as to make the port, use the main menu to select

**Connectivity > Port > Make port**

In the prompt bar, enter the following into the dialog boxes (use TAB to move between fields)

For an input port,



**Port Type = Signal; Direction = in; Port Name = in**, then click OK. (Use *in* rather than *in1* which is shown in the figure).

Repeat for the output port (unselect the input first!) setting **Port Type = Signal; Direction = out; Port Name = out**, then click OK

We also need to make ports of our power and ground rails. To make the VDD power port, select metal1 layer across the top of your cell and go to  
Objects > Make > Port

and enter the following:

**Port Type = Power; Direction = In; Port Name = VDD**, then hit return.

Repeat for the ground power port selecting the metal1 layer at the bottom of your cell and naming it **ground**.

Finally, unselect everything on the canvas by hitting the F2 key.

### 3.3.10. Adding Property Text

Following steps similar to adding ports, add Property Text to the input, output, and power ports. Select one port at a time and the select

Easy Edit > Property Text

Add text to your layout, including port names, etc. Use the same names as you used for the schematic ports, namely **in, out, VDD, ground**. You can vary the set the size of the text by clicking on the Options tab and entering a value in units of 'grids'. 5 is recommended. You should keep the default layer setting (or bad things might happen....)

### 3.3.11. Setting the cell origin:

When we instantiate cells into higher-level layouts, we need to have a reference point for the cell. This is the 'cell origin'. To make life easier, it is recommended that you set the origin of all cells to the same general location. From the main menu, select

Context > Set cell origin

The mouse pointer changes to + form and you must click on the spot where the origin is desired. Set the origin of your inverter to be the bottom left-hand corner of the ground rail metal1 layer (where it meets the p-select layer placed around the substrate tap).

Very Important: Once you instantiate a layout cell into a higher-level cell, you should NOT change the origin, as this will cause the cell to shift within the higher-level cell, thereby disrupting any connections you would have made using this cell as a component.

## **3.4 Checking your Layout**

During this tutorial, you will be asked to jump down to this section and complete a few steps before going back to continue the main exercise. However, after you complete the steps in these earlier steps, you should go through the DRC check one more time and then complete the LVS steps outlined below before continuing to the Extraction step.

### Design Rule Checker

From the main menu, select

**Checking > DRC (IC rules)**

to begin a rules check. The number of DRC errors will appear at the bottom of the screen as '**total results**'. A description of the errors can be obtained by selecting

**Checking > First Error**

then, after the first error, select

**Checking > Next Error**

For each error, the area under violation is highlighted and described at the bottom of the screen. Correct errors by moving/editing layers and conforming to the DRC rules. Continue corrections and DRC checking until you have **no** rule violations.

### LVS( Layout Vs Schematic):

The LVS process compares the layout with the schematic to *verify* your layout matches. In the main **IC Palette** select

**IC Trace (M)**

Then press

**Load Rules**

and indicate the path to the rules file as follows (this may already be set up from an earlier step):

```
/usr/local/mgc_tree/ADK/technology/ic/ami05.rules
```

then click OK.

While still in the IC Trace (M) palette, select

**LVS**

and enter the name of the schematic to which you will compare your layout. Here, you should enter `inv/sdl`

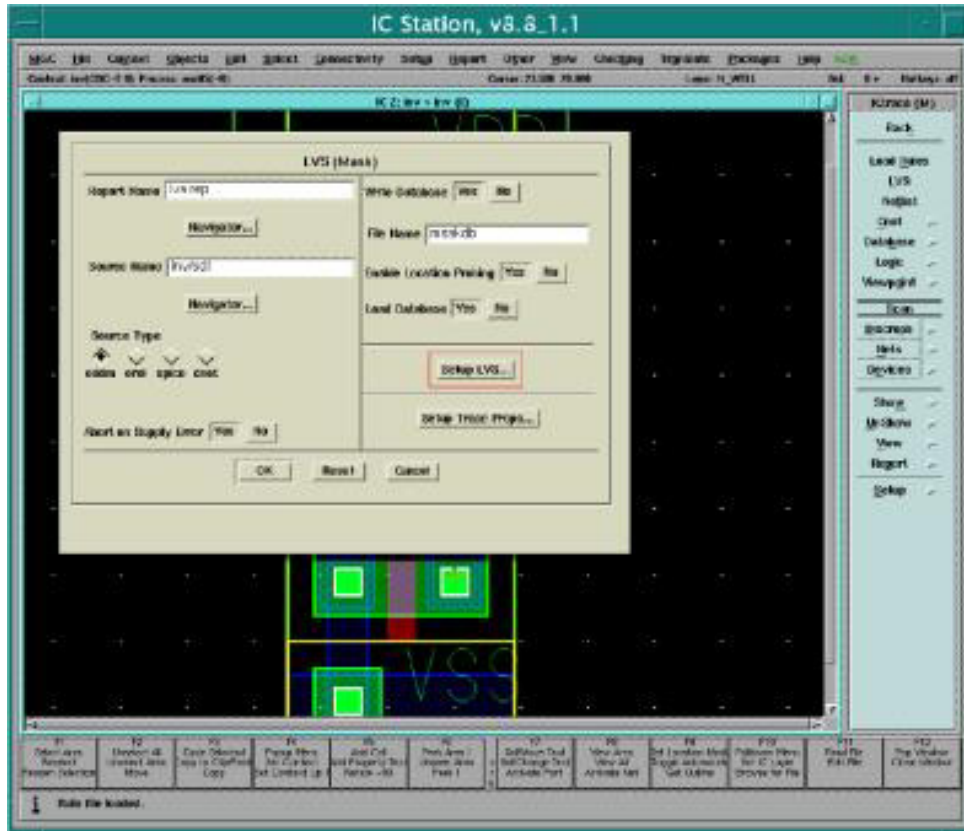
Or, you will need to point to the viewpoint file you created while using Design Architect.

Leave all other options as their default values. Click OK.

The LVS checker will begin comparing your layout to your schematic. When this is done, you will see that 'mask results database loaded' appears at the bottom of the screen. Select the following on the IC trace(M) palette:

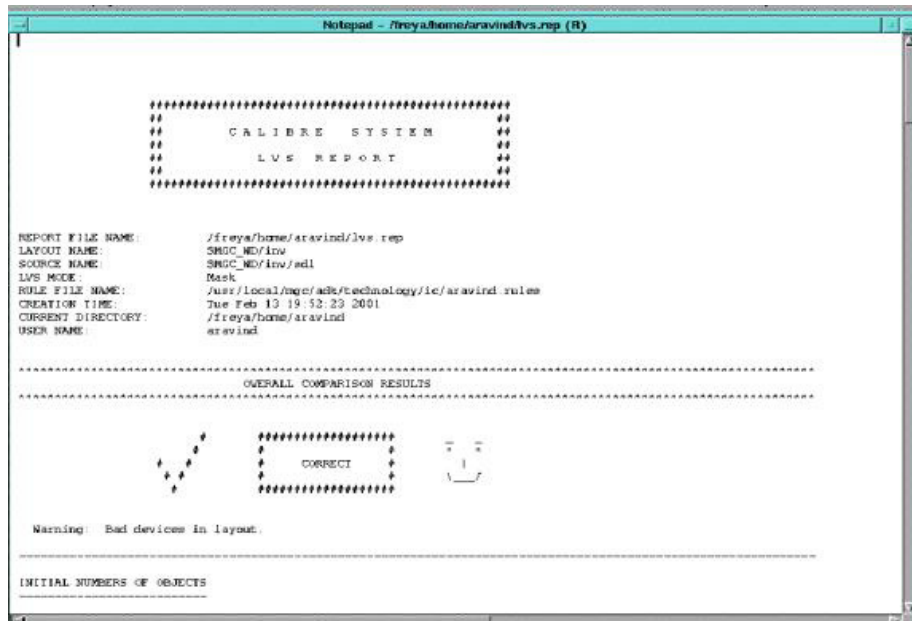
Report > LVS

A successful LVS shows up a smiley face with a CORRECT sign as shown in the figure below. If there are errors, the information in this report will help you track and fix those errors. Fixing errors will involve moving/modifying/adding layers, checking/correcting port definitions, etc. Learning how to track and fix LVS problems is a major part of learning these CAD tools (and one that takes practice and time to become proficient).



Before you finish, you MUST PASS LVS and get a smiley face.

Very Important: be sure to close the LVS report before running another LVS. Otherwise, the old report will not be overwritten and you will see the old LVS report when you open it. (It's not a bug, it's a feature...)



Although you must fix all errors, you can ignore the warning about bad devices in the layout.

Once you have successfully passed LVS, you should save your cell. Select the following button options and you are done with this exercise.

**File > Cell > Save Cell > Current Context**

The next step is to take what you have learned here, and practice it by working on the project artifacts.

#### **4. Layout Editing Tips**

##### Easy Edit Menu:

Select Easy Edit from the IC Palettes menu. This causes the IC Palette to be replaced by an edit menu, which contains many editing functions that you will need. Many of these functions are explained in the following paragraphs. Additional edit functions can be found in the Expert Edit palette, such as the Move Edge tool described below.

(We use the abbreviation 'LMB', below, to refer to 'left mouse button'.)

##### **Add Shape:**

Click on Shapes in this menu. A pop up dialog box appears on the bottom of the layout window. It indicates the current command that has been invoked. On the layer palette in the upper right hand corner of the IC Station window, click on the metal1 (CMF) layer with the LMB. This selects metal1 as the current layer for the next shape to be drawn. In the layout edit window you now see that the cursor has change shape to a cross. Keeping the LMB pressed, drag the mouse until you complete drawing the shape. You should see a blue highlighted rectangle, indicating the this object is the current active object (in an editing context). To unselect this shape, press the F2 key. To reselect this shape place the cursor on the shape and press the F1 key.

In general, F1 selects the nearest unselected shape whereas F2 unselects all selected objects. To clearly identify a selected shape it is always highlighted.

##### **Delete:**

If you erroneously enter an incorrect shape, select it and then click the LMB on Delete in the Easy Edit menu. Click on OK in the dialog box that appears at the bottom of the window. This causes the selected shape to be deleted. You can also simply hit the Delete key on your keypad and everything selected will be deleted.

##### **Undo:**

You can undo the previous operation by clicking on the Undo in the palette. If you place your mouse is over the layout window, just type 'undo' and hit Enter to get the same function.

##### **Copy:**

Select the shape to be copied. Then click on Copy in the Easy Edit menu. Click on OK in the dialog box and you should then see a ghost image of the selected shape, which is dragged about with the mouse. Place it at the correct location and click the LMB to fix the position of the copy. You will still see the ghost image and so, if you wish, you can copy it to yet another place. When you are done copying press the F2 key and all copied shapes will appear in their new locations.

Rel Copy is used to copy the selected shape for the known displacement along X and Y-axes. Select the shape, click 'rel copy', fill in the offset values and click OK.

**Move:**

This feature is similar to copy except that the original shape does not stay in place. Place F2 at the end of the move to fix the location of the shape. Rel Move can be used if you desire to move along known displacement along X and Y axes. Select the shape, click 'rel move' and fill in the offset values and click ok.

**Notch:**

This feature is used to edit shapes that are in the right place but are of the wrong shape or size. Select a shape using F1. Assume that the shape is smaller along one dimension than it needs to be. Click on Notch in the Easy Edit menu. Click OK in the dialog box. Now, position the cursor on the boundary of the selected shape and keeping the LMB pressed, drag the cursor to form a box that represents say the additional size that the shape needed to be. Release the mouse button and you should see that the shape has now increased to the desired size.

Similarly, you can reduce object size, or add different shapes, etc., using the Notch command. One thing to keep in mind is that before notching, i.e. dragging the mouse with the left button pressed, you must position the mouse on the edge of the selected shape.

**Stretch:**

This feature is used to increase or decrease dimension of an edge. Click on Stretch in the Easy Edit menu. Select an edge. Drag the edge with your LHM to the desired position.

**Flip:**

Any shape can be flipped about any axis. Select the layer or an area, click flip in the easy edit palette and with LHM presses, draw the axis about which the shape needs to be flipped.

**Align:**

Select the area to be aligned to a target object. Click 'align'. This changes the mouse pointer, that when clicked at the target object pops up a window as shown. Select the directions of source and target objects to be aligned and if needed, fill in the offset value. Click ok.

**Rotate:**

Select the shape to be rotated and click 'Rotate'. A dialog box appears at the bottom of the screen and the angle to which the selected shape to be rotated is to be written. Click ok.

Expert Edit menu:

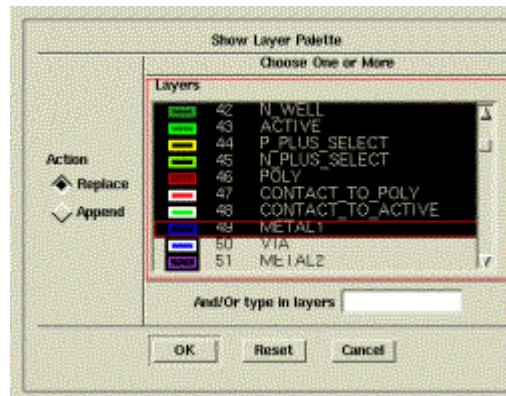
A useful feature in the expert edit menu is the move edge function, **MVED+**. It functions as both stretch and move command. By selecting a edge of a polygon, the MVED+ function as "stretch". On the other hand, by selecting the whole polygon, MVED+ function as "move". Once you turn on MVED, clicking on the screen will no longer select the nearest object, but it will select the nearest edge. It's confusing at first, but many people find a combination of MVED and notch will do almost all edit functions needed.

Using the Layer Palette:

Adding shapes is one of the most common activities, but selecting layers from the ADD SH dialog box can be cumbersome. To ease this task, you can add a **layer palette** at the right hand top corner of the screen which contains all of the layers you need and can be easily edited to add/remove other layers. From the main menu, select

**Other > Layers > Show layer palette**

In the dialog box that appears you will see a list of all the



layers for the chosen process. Scroll down the list to find the layers you will need. First, select layer number 42 i.e. N\_W, click it and by holding the control key (on the keyboard), select the other layers you need (from layer number 43 to 49). Once all the layers from 42 to 49 are selected, click 'OK'.

If you happen to miss selecting few layers in your first attempt or you need any additional layers, you can always go to

**Other > Layers > Append to the layer palette**

which opens up the same dialog box and you can add additional layers to the existing palette by selecting them as explained above and clicking 'OK'.

Once the layer palette is chosen, it appears at the right hand top corner of the screen above the easy edit menu as shown here to the right.

If at any point you wish to hide/delete the layer palette, go to

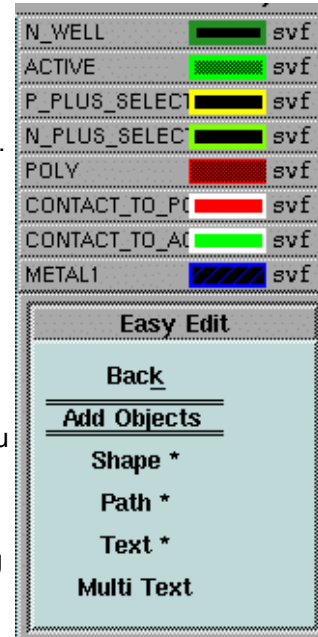
**Other > Layers > Hide layer palette**

and it disappears.

The layer palette is used to pre-select the layer that will be drawn when you use the

**Easy Edit > Shape**

command to add a shape to your layout window. Just click on the desired layer from the layer palette, click on *Shape* in the palette, and start drawing the layer you want.



Useful Macros:

To use any of these commands, simply type them in the cell window. A prompt bar will appear with your command in it.

**Function Description**

- pc Place a poly contact; places a poly contact centered at the current cursor position.
- pp Place a port contact; creates a port and places it where you click.
- nwc Place an n-well contact; creates and places an n-well contact on the standard cell power rails.
- pwc Place a p-well contact; creates and places p-well contact on the standard cell power rails.
- p Place a poly path of width 2 (minimum width); Prompts you to place a poly path.
- m Place a metal1 path of width 3 (minimum width); Prompts you to place a metal1 path.
- v Move unconstrained; Moves the selected object(s).
- ec5 Lumped, mask extraction for AMI 0.5; This command scripts the extraction to a specific location that probably does not exist at your site. Modify this command if you wish to use it.
- rab1 Remove metal1 blockages; This command will remove all metal1 blockages in your cell.
- s5 Set cell process to AMI 0.5
- cp Checkpoint cell; save the cell and then reserve the cell.
- dup Delete unplaced ports; If LVS reports unplaced ports but you see that they are all placed from your schematic, the database might have duplicate ports. This command will remove them.

## 5. Hierarchical Design

This section contains information about creating designs in Mentor Design Architect and IC Design tools using a hierarchical approach. Hierarchy in circuit design refers to the creation of higher level cells based on lower level cells (assuming we are building our design units bottom-up). For example, if you create a cell that is composed of inverters and NAND gates, you can *instantiate* (add) your previously designed inverter and NAND cells rather than recreating them in the higher level cell. This section provides some commands that are necessary to create hierarchical designs with instantiated cells.

### 5.1 Hierarchy in Schematic Capture (Design Architect)

Once you launch DA and open a New Sheet for your new higher-level cell

File > Open > Sheet

you can start adding the cells you have previously created. From the schematic\_add\_route palette, select

Choose Symbol

This opens up a dialog box in which you can select the symbol for the desired lower-level cell. Scroll down to locate the cell/symbol you need to add. Select it and click OK. A ghost image of the symbol will appear and should be dragged and placed where it's needed in your new cell.

If desired, you can look down into the symbol to see the schematic of the instantiated (added) cell. This action is called 'peeking'. To peek the symbol, select it and press Control+F8.

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### 5.2 Hierarchy in Layout (IC Station)

#### 5.2.1 Add Cell:

Any previously created cell can be added to the layout of a higher-level cell with the Add Cell function. With the mouse pointer on the layout window, press F5. An 'add cell' dialog box pops up and you need to enter the layout cell name, e.g., *inv*. You must enter the complete path if the cell to be added is in a different directory than your current directory (from which you launched IC). Click OK and you will see a ghost image of the cell with an outline box. Place the cell where you want it by clicking on the layout window. Cells will be placed with their origin (recall the Set Origin command) at the positing where you click to place the cell. Press F2 to unselect the added cell. Notice that only the ports of the cell are visible at this time.

You can moved added cells just like any polygon in IC station and the entire cell will move. To move these cells, select them and from easy edit menu, use 'move' function, or use the function keys. As all these basic cells have been assigned pitch match of 50L or 50λ, the VDD and VSS/GND rails should align. If you set cell origin (as recommended) at the bottom left corner of GND rail, it's quite easy to align the power the rails.

#### 5.2.2 Peeking Cells:

To view all of the layers within an added cell, select the cell (the outline and ports are selected) and press control+F6. Press F2 to unselect all. Note that although you can see the lower-level layers, you cannot edit them from this cell (there is a way, but for now, assume you can not). To edit a lower-level cell you should open that cell and edit it there. However, be warned that any changes you make in a lower level cell will change anywhere you have used that cell in the design hierarchy. For this reason, it is highly recommended that you do NOT edit lower-level cell layouts once that layout is completed.

### 5.2.3 Making Arrays:

If you need to duplicate an added cell over one or two dimensions, first select the added cell. Then, from the main menu select

Objects > Make > Arrays

A dialog box will show up at the bottom of the screen. Enter the # of rows and columns that you want the array to be. Click on OK and the new structure will be shown in the layout.

