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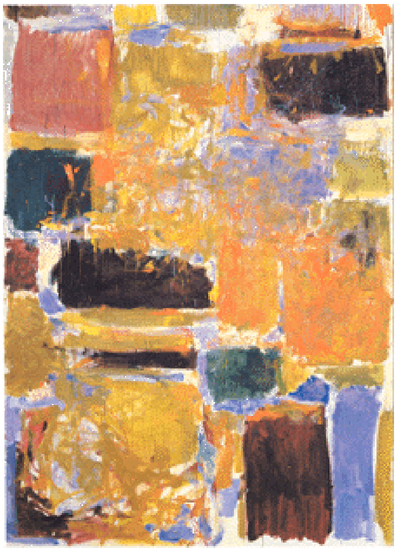

CSCE 613 – Week 10
Fall 2005

CMOS VLSI Design

Analysis Examples

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Topics of Week 10

- **Text examples – We'll look at these examples and show how they fit together as part of an overall design analysis problem (Rabaey et al., Ch 4).**
- **A layout example – we take a layout circuit application and attempt to apply the knowledge we've learned to date (in preparation for homework and an upcoming exam).**
  - **Layout geometry, topology and design rules.**
  - **Device parasitics analysis.**
  - **Wire parasitics analysis.**
  - **Wire delay analysis.**
  - **Geometry scaling: 0.5 -> 0.25: how do we modify our design?**
- **We take the basic topology and rules from Weste et al. (only because Rabaey et al. doesn't give us a good rule set to work with), but we'll use the analysis model from Rabaey et al. (Ch4, Ch5).**

Rabaey et al. Ch4 - Analysis Examples

- Example 4.1, p. 144.
  - Capacitance of metal wire
  - Factor of 2x for Cfringe calculation due to both sides of wire cylinder “fringing”.
  - Uses Table 4-2, p. 143, and Table 4-3, p. 144.
- Example 4.2, pp. 146-147.
  - Computing total resistance from R ▯ .
  - Comparing resistance of metal vs. Poly lines.
- Examples 4.3, p. 148.
  - Resistive skin effect analysis.
  - Plotting skin effect to determine at what line widths it becomes noticeable.
- Example 4.4, p. 150.
  - Inductance of metal wires of different widths.
  - Calculate $c_{pp} + c_{fringe}$ (also using 2x factor for c_{fringe} from Ex 4.1).
  - Identifying at what operating frequency and given wire widths we start to see inductance effects.
- Example 4.5, p. 152.
  - Lumped capacitance of wire, using Kirchoff’s law, Ohm’s law, RC time constant.
- Example 4.6, p. 154.
  - Elmore calculation of RC-induced wire delay of tree-structured network.

Ch 4 - Wiring Capacitances (0.25 μm CMOS)

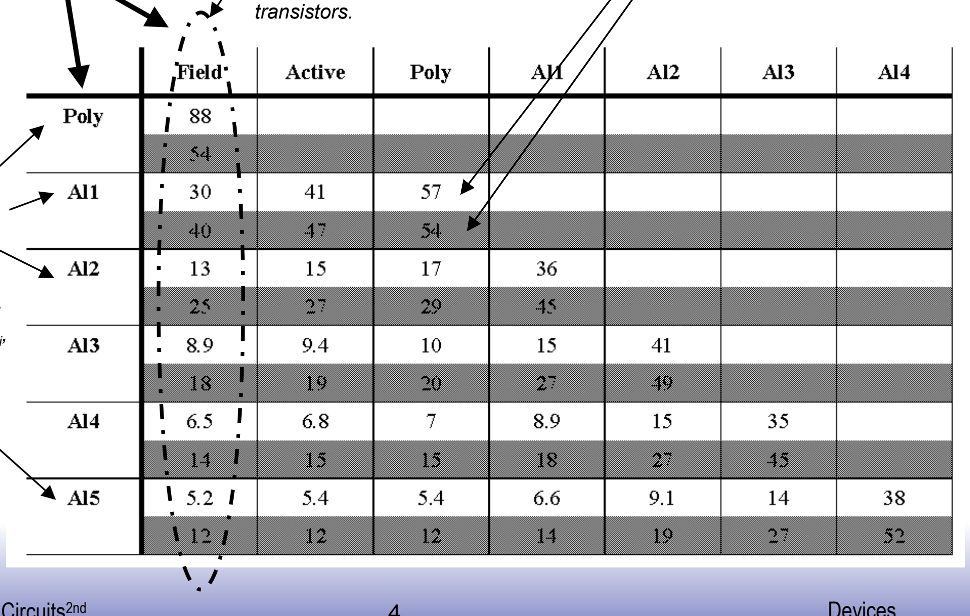
Table rows are capacitor’s “top plate. Table columns are its “bottom plate”.

Use the Field values for C terms when placing wires over thick field oxide (SiO2) that isolates different transistors.

C_{pp} values in upper row. C_{fringe} values in lower, shaded row.

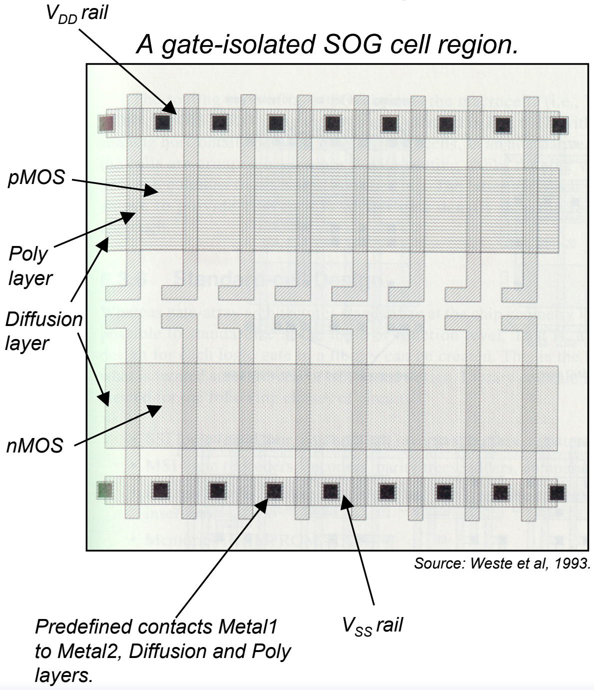
Process supports 1 layer Poly and 5 layers Metal.

First 4 metal layers Use same H and t_{di}, But 5th layer has $H_{m5} = 2H_m$ and $\varepsilon_{di5} > \varepsilon_{di}$.



	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

SOG Layout Design Problem-1

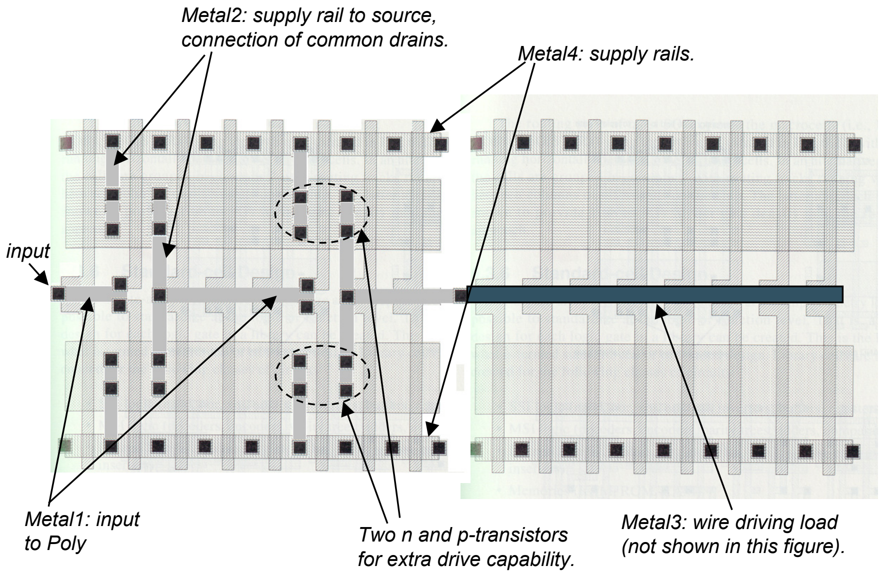


A gate-isolated SOG cell region.

Source: Weste et al, 1993.

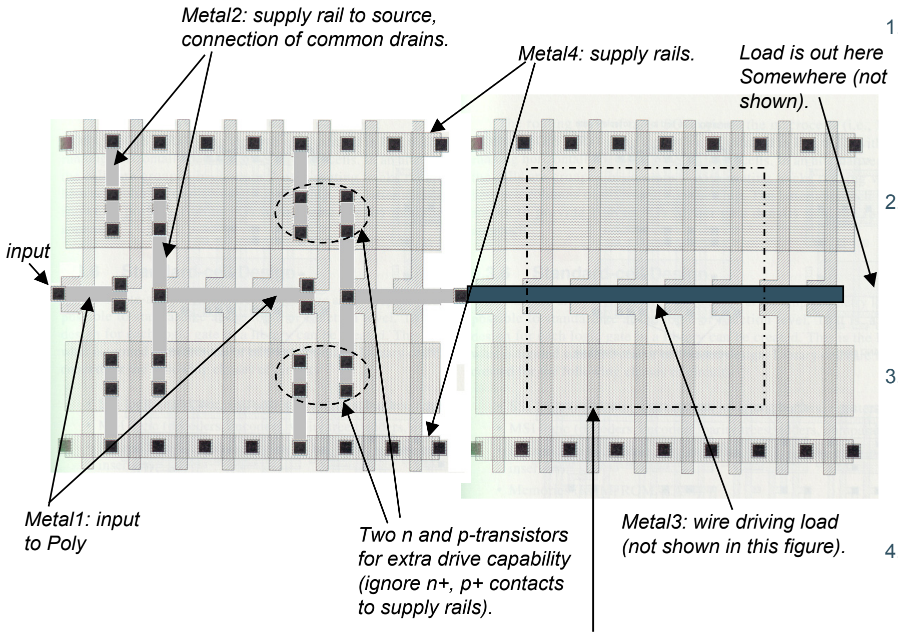
- We'll use a base substrate formed using the Gate isolated SOG array structure.
- We'll assume the 0.5μ process and design rules presented in Weste et al. for the initial part of the problem.
- We'll assume specific parameters for pMOS and nMOS transistors for the inverter, and don't show the wells on the layout diagram.
- We'll make some additional assumptions about the wire layers (according to Weste et al.) and derive the parasitics and delay relationships using Rabaey et al.

SOG Layout Design Problem-1



- Two Inverters in series – Buffer
- *Metal1* runs horizontal: connecting to Poly from input, inverter output to next input.
- *Metal2* runs vertical: common drain connection, and supply rail to Active diffusion (we ignore the p+/n+ connection of bulk to supply).
- *Metal3* runs horizontal: provides wire between buffer and load.
- *Metal4*: supply rails (not to scale).

SOG Layout Design Problem-1



Metal2: supply rail to source, connection of common drains.

Metal4: supply rails.

Load is out here Somewhere (not shown).

input

Metal1: input to Poly

Two n and p-transistors for extra drive capability (ignore n+, p+ contacts to supply rails).

Metal3: wire driving load (not shown in this figure).

Another circuit exists in this region (not shown), so we have to route over it. Can we do this?

- ❑ Questions:

1. Which design rules must we use to check the device layout?
2. How do we evaluate the sizes of our inverter transistors (ratio)?
3. How do we calculate the device capacitance and resistance?
4. How do we bring the calculations for parasitics and delay into the analysis?

CMOS 0.5μ Design Rules (redux)

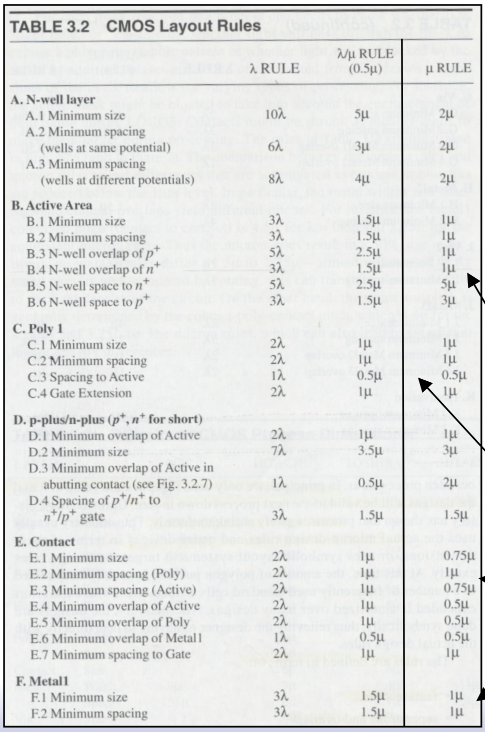


TABLE 3.2 CMOS Layout Rules

	λ RULE	λ/μ RULE (0.5μ)	μ RULE
A. N-well layer			
A.1 Minimum size	10λ	5μ	2μ
A.2 Minimum spacing (wells at same potential)	6λ	3μ	2μ
A.3 Minimum spacing (wells at different potentials)	8λ	4μ	2μ
B. Active Area			
B.1 Minimum size	3λ	1.5μ	1μ
B.2 Minimum spacing	3λ	1.5μ	1μ
B.3 N-well overlap of p^+	5λ	2.5μ	1μ
B.4 N-well overlap of n^+	3λ	1.5μ	1μ
B.5 N-well space to n^+	5λ	2.5μ	5μ
B.6 N-well space to p^+	3λ	1.5μ	3μ
C. Poly 1			
C.1 Minimum size	2λ	1μ	1μ
C.2 Minimum spacing	2λ	1μ	1μ
C.3 Spacing to Active	1λ	0.5μ	0.5μ
C.4 Gate Extension	2λ	1μ	1μ
D. p-plus/n-plus (p^+, n^+ for short)			
D.1 Minimum overlap of Active	2λ	1μ	1μ
D.2 Minimum size	7λ	3.5μ	3μ
D.3 Minimum overlap of Active in abutting contact (see Fig. 3.2.7)	1λ	0.5μ	2μ
D.4 Spacing of p^+/n^+ to n^+/p^+ gate	3λ	1.5μ	1.5μ
E. Contact			
E.1 Minimum size	2λ	1μ	0.75μ
E.2 Minimum spacing (Poly)	2λ	1μ	1μ
E.3 Minimum spacing (Active)	2λ	1μ	0.75μ
E.4 Minimum overlap of Active	2λ	1μ	0.5μ
E.5 Minimum overlap of Poly	2λ	1μ	0.5μ
E.6 Minimum overlap of Metal1	1λ	0.5μ	0.5μ
E.7 Minimum spacing to Gate	2λ	1μ	1μ
F. Metal1			
F.1 Minimum size	3λ	1.5μ	1μ
F.2 Minimum spacing	3λ	1.5μ	1μ

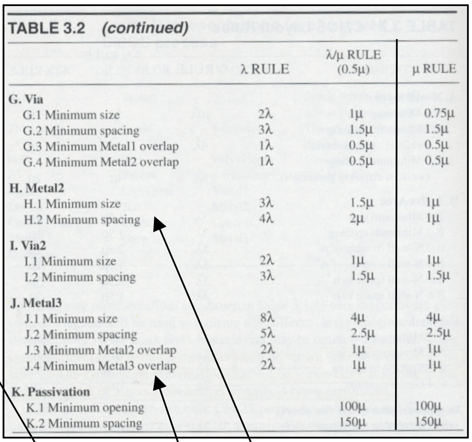


TABLE 3.2 *(continued)*

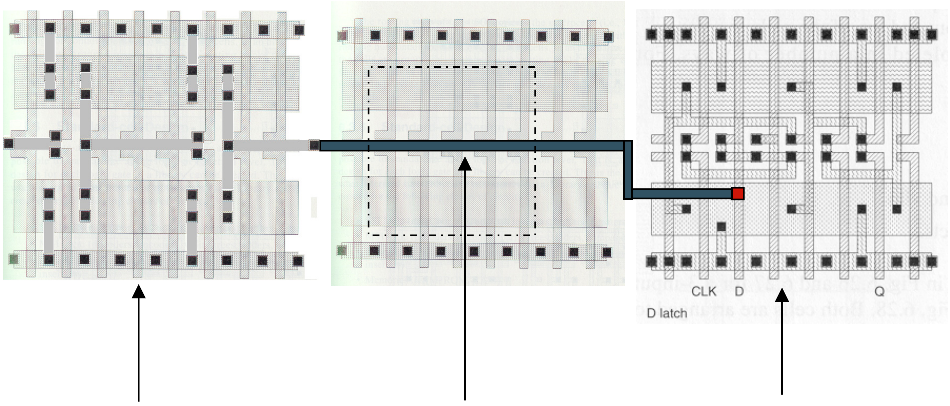
	λ RULE	λ/μ RULE (0.5μ)	μ RULE
G. Via			
G.1 Minimum size	2λ	1μ	0.75μ
G.2 Minimum spacing	3λ	1.5μ	1.5μ
G.3 Minimum Metal1 overlap	1λ	0.5μ	0.5μ
G.4 Minimum Metal2 overlap	1λ	0.5μ	0.5μ
H. Metal2			
H.1 Minimum size	3λ	1.5μ	1μ
H.2 Minimum spacing	4λ	2μ	1μ
I. Via2			
I.1 Minimum size	2λ	1μ	1μ
I.2 Minimum spacing	3λ	1.5μ	1.5μ
J. Metal3			
J.1 Minimum size	8λ	4μ	4μ
J.2 Minimum spacing	5λ	2.5μ	2.5μ
J.3 Minimum Metal2 overlap	2λ	1μ	1μ
J.4 Minimum Metal3 overlap	2λ	1μ	1μ
K. Passivation			
K.1 Minimum opening		100μ	100μ
K.2 Minimum spacing		150μ	150μ

Source: Weste et al, 1993.

In our design example, we'll use the following Sets of rules: (1) Active, (2) Poly1, (3) Contact, (4) Meta1, (5), Metal2, (6) Metal3 (except J.3 will be for Metal1 rather than Metal2, given that Metal1 and Metal3 are both aligned horizontally).

SOG Layout Design Problem-1

To effectively analyze this problem, we need to first analyze the devices, then the wires, using the models developed in Rabaey Ch4, and with Inverter information from Ch5. Note that this process of analysis and layout design is iterative: we'll make a 1st pass to collect initial data, then follow-up with a 2nd pass to modify initial assumptions.

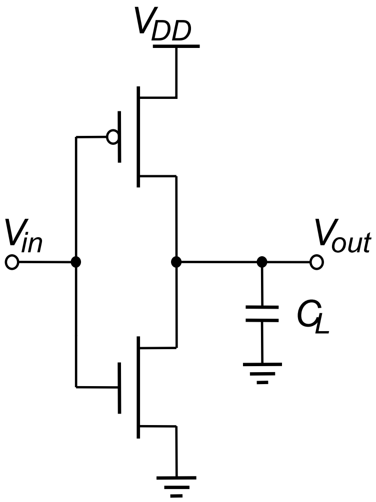


We'll use the model and analysis developed in Chapter 5 Rabaey to come up with relevant parameters to guide layout analysis.

We'll use the models from Rabaey Chapter 4 to analyze the long-line effects of the wire interconnect between driver and load for routing.

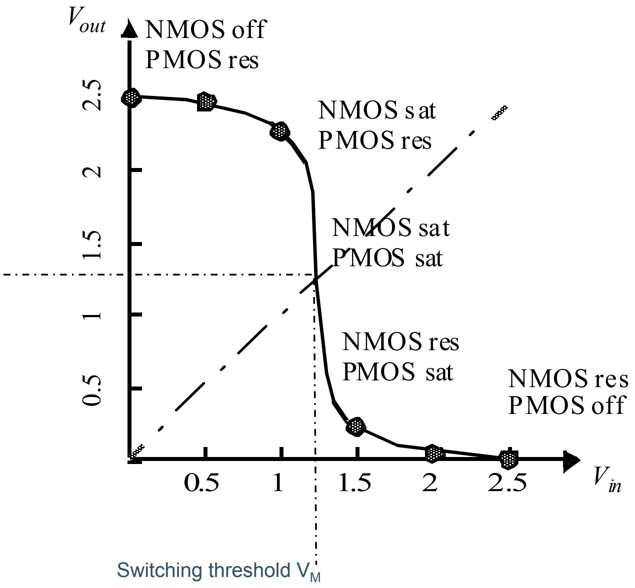
We'll use some modeling from Rabaey Chapters 5&6 to assess the loading and fan-out impact on wire modeling.

The Device – CMOS Inverter (Rabaey Ch5)



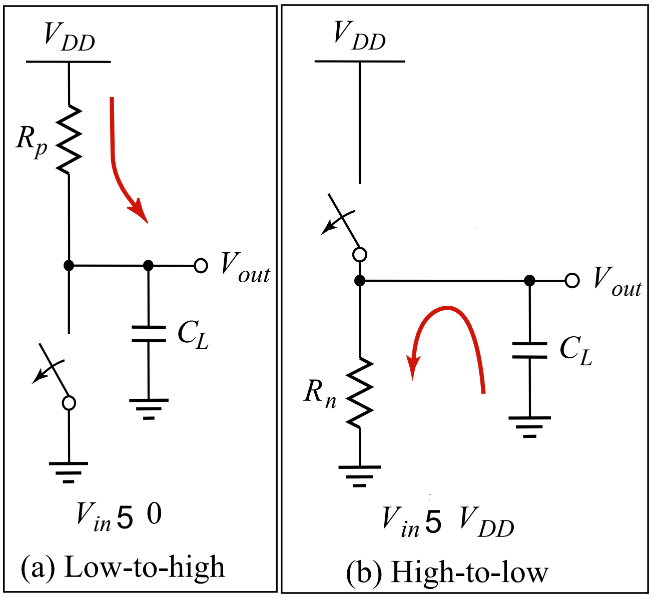
- Static (steady state) properties
  - High and low output levels are V_{DD} and GND.
  - "Ratio-less" nMOS and pMOS transistors (logic levels not dependent on transistor sizes)
  - Finite R_S resistance between the driving logic source (V_{DD} or GND) and output.
  - Low Z_S output impedance, so less sensitive to noise or disturbances.
  - High R_L input resistance to the inverter (we'd see this in the 2nd inverter in the Buffer chain of our example).
  - No direct path between V_{DD} or GND.

The Device – CMOS Inverter (Rabaey Ch5)



- Dynamic (switching) properties
  - Using the Voltage Transfer Characteristic (VTC) curve: superimpose those of nMOS and pMOS devices.
  - V_{DD} = 2.5v
  - The VTC shows a narrow transition zone (I.e., fast switching), due to high gain during switching transient.
  - Both transistors are on and in saturation mode. Small change in V_{in} results in large V_{out} variation.
  - Switching threshold, V_M is at the point where $V_{out} = V_{in}$.

The Device – CMOS Inverter (Rabaey Ch5)

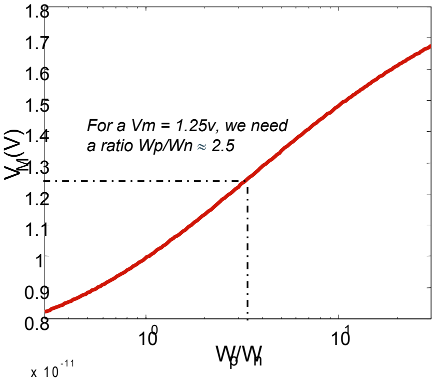


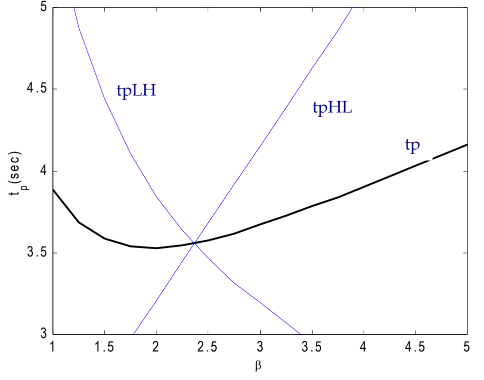
(a) Low-to-high

(b) High-to-low

- Dynamic (switching) properties
  - Transient response dominated by Capacitance C_L, composed of (1) drain-diffusion capacitance of transistors, (2) wire capacitances, (3) input capacitance of fan-out gates.
  - Gate response time (L-H): time to charge the capacitor C_L through resistor R_p.
  - Gate response time (H-L): time to discharge the capacitor C_L through resistor R_n.
  - Prop delay $t_p \propto R_p C_L$ (time constant) .
  - Fast inverter is built by: (1) keep C_L small, (2) decrease device on-resistance (increasing W/L ratio).

The Device – CMOS Inverter (Rabaey Ch5)



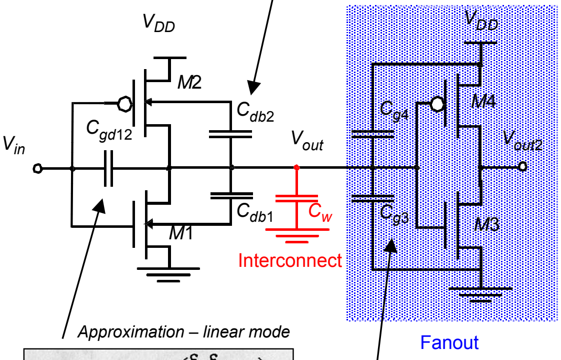


- Transistor sizing
  - The point V_M on the VTC curve is most desirable for operation at $V_{DD}/2$ = 1.25v.
  - This provides comparable values for low and high noise margins.
  - Driving strength ratio r: compares relative driving strengths of pMOS and nMOS transistors.
  - For VM = $V_{DD}/2$, r ≈1 ⇒ pMOS device size $(W/L)_p = \beta(W/L)_n$, or $\beta = W_p / W_n$.
  - Assumption for 0.25 micron process is that the devices are in velocity saturation (p. 185 Rabaey uses equs. 5.4 & 5.5 with V_{DSAT} for p and n devices).
  - NOTE: variations in the device sizes and their ratio β have minor impact on V_M (so W_p could be closer to W_n).

The Device – CMOS Inverter (Rabaey Ch5)

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)}[(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$



Approximation – linear mode

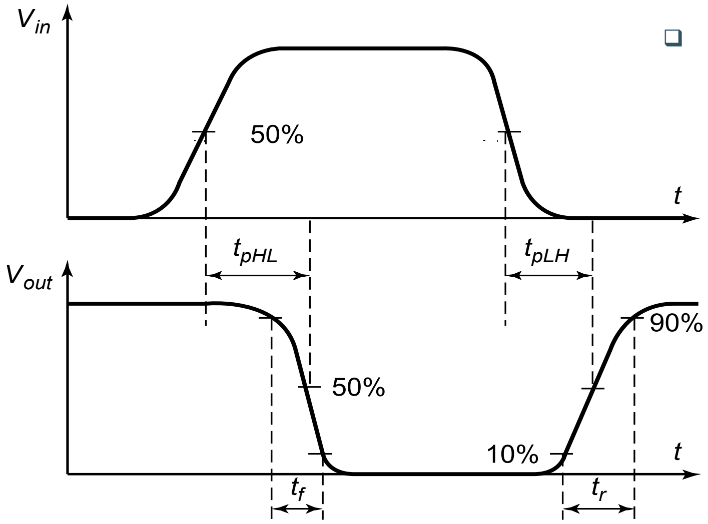
$$C_{gd} = C_{gs} = \frac{1}{2}\left(\frac{\varepsilon_0 \varepsilon_{SiO_2}}{t_{ox}}\right)A.$$

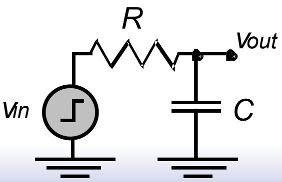
Source: Weste et al., 1995.

Only consider capacitance at the gates, ignore that at the channel (~10% error).

- Computing Capacitances
  - Assume all device capacitances are lumped into a single capacitor, C_L.
  - Assume that input V_{in} is driven by an ideal voltage source (step, $t_r = t_f = 0$).
  - We have composite C_L: (1) gate-drain, (2) diffusion, (3) wiring, and (4) fan-out load gate capacitances.
  - *Gate-Drain* C_{gd}: having identical but opposite voltage swings at both its terminals, we model by a capacitor to GND with twice the value of original, i.e. $2C_{gd}$. See Weste et al. equ., below.
  - *Diffusion* C_{db}: drain to bulk C_{db} is due to reverse-bias *pn*-junction. We model linearly using factor K_{eq} with junction capacitance per unit area (under zero bias), C_{j0}. (Equ. 5.13). We have two components: (1) *bottom plate*, and (2) *side wall* (see Lecture 12 notes).
  - *Wiring* C_W: wire model depends on W, L of wires, line length (Ch4 model), and number of fan-out gates.
  - *Fan-out* C_g: load capacitance is sum of C_g on transistors at the load (Equ. 5.15, p.196).

The Device – CMOS Inverter (Rabaey Ch1)





$$v_{out}(t) = (1 - e^{-t/\tau})\, V$$

$t_p = \ln(2)\, \tau = 0.69\, RC$

- Inverter Delay
  - Measure propagation of signal from L-H and H-L, between V_{in} and V_{out}, using 50% ($V_{DD}/2$).
  - Measure rise and fall times on V_{out}, ranging between 10%-90% V_{DD}.
  - Approximate inverter delay by using the first-order RC network (lumped parameter model, Ch 5), solving for time constant, then getting prop. delay.
  - We'll solve for t_{pLH} (pMOS) and t_{pHL} (nMOS), finding the transition prop. delays in terms of CL and R_{eqp} and R_{eqn}. These will follow the W_p/W_n ratio of transistors, based on V_M.
  - Total t_p is average of t_{pHL} + t_{pLH}.