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CSCE 613 – Week 6 Fall 2005

CMOS VLSI Design

Introduction to CMOS Wire

Adapted/extended by James P. Davis, Ph.D.
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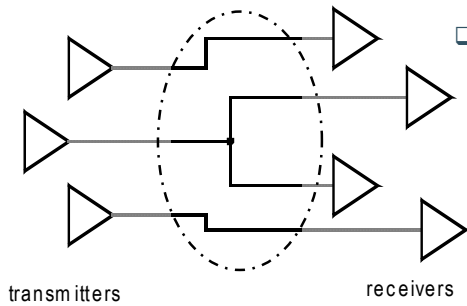
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Devices

Topics - Week 6

- Interconnect between MOS transistor structures – the “wire”, in terms of behavior, function and structure (materials from Rabaey et al.)
 - Coverage from Rabaey et al., Chapter 4, §4.1 - §4.3.2, pp. 136 - 148, 4.3.3, 4.4.1 - 4.4.5, pp. 148 - 169.
 - Examples from Ch4 text – the progression of modeling results for the .25 micron CMOS process.
- Capacitance revisited, modeling and assumptions for the wire (this is a review, reformulation and extension of notes presented earlier from Weste et al.)
- Resistance revisited, modeling and assumptions for the wire (this is a review, reformulation and extension of notes presented earlier from Weste et al.). We also consider effects of switching frequency.
- Inductance on the wire, which we consider at large wire sizes with low resistance, and high switching frequencies.

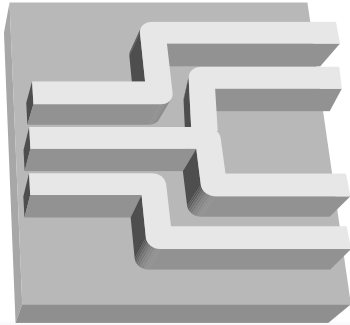
Introduction to The Wire



transmitters

receivers

schematics

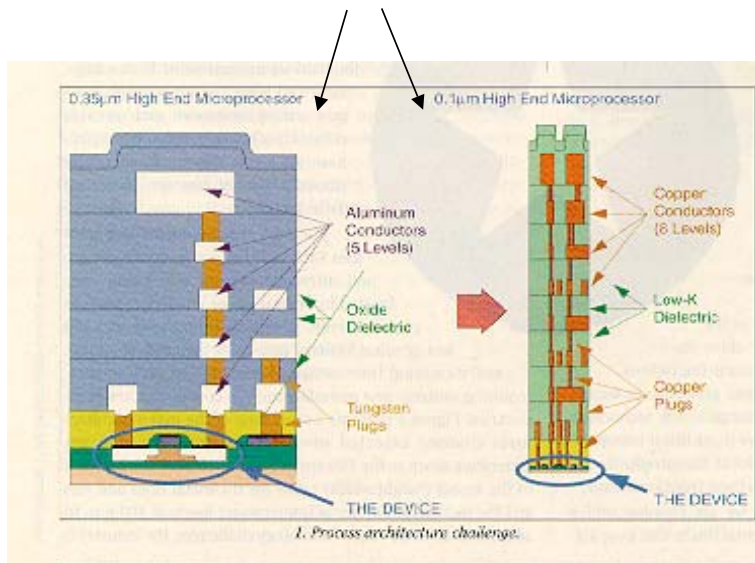


physical

- **Scaling of interconnect versus devices**
 - As we scale CMOS devices and their interconnect, the effects of *parasitics* on the wires becomes more pronounced, particularly in scaled circuits running at higher speeds.
 - Wires scaling effects dominate in areas of speed, power consumption, reliability (noise immunity).
 - Larger die sizes exacerbate the problem, as line lengths get longer.
- **Effect of “parasitics” on CMOS circuits**
 - Increase propagation delays, and decrease transistor performance.
 - Affect on energy dissipation & power distribution throughout the circuit.
 - Create additional sources of noise.
- **Basic wire modeling abstraction**
 - We only use a few dominant parameters.
 - Each wire in bus network connects “transmitter(s)” to “receiver(s)” via a chain of wire segments w/ length and geometry.

Interconnect Impact on Chip

Comparing 0.35 μ versus 0.1 μ CMOS processes, noting their differences in geometry, specifically pertaining to number of layers of interconnect.

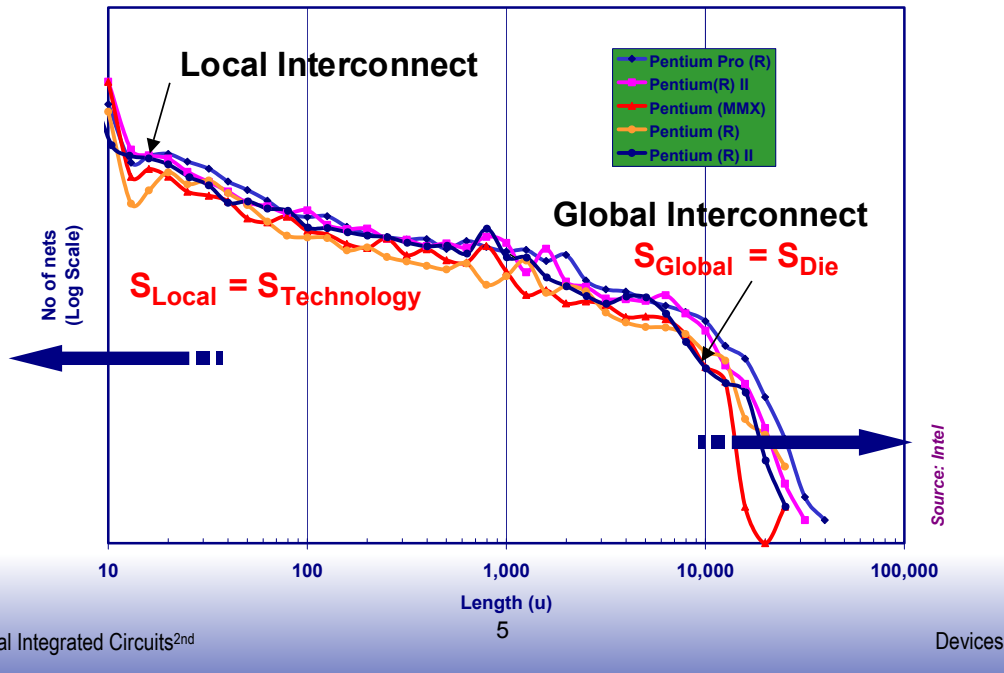


□ Geometry Layering

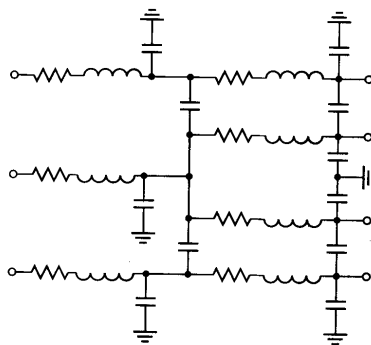
- As we scale processes, we also add more process layers to the circuit geometry.
- We still have single diffusion and poly layers.
- We have many more layers of metal, sandwiched between layers of insulator.
- It is this more aggressive geometry structuring, coupled with smaller wire feature size versus length, that makes wire modeling a challenge.
- New materials are part of the solution.

Nature of Interconnect – Real Data

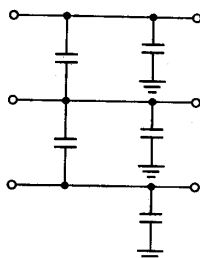
Here, we are comparing the relative number of nets required for local versus global interconnect for Pentium® class of CMOS devices (with ~30-40M transistors) as a function of actual line length. Technology scaling is facilitating smaller wire size, while increases in die size facilitate longer line lengths—the source of greater parasitic impact.



Wire Modeling-1



All-inclusive RLC model

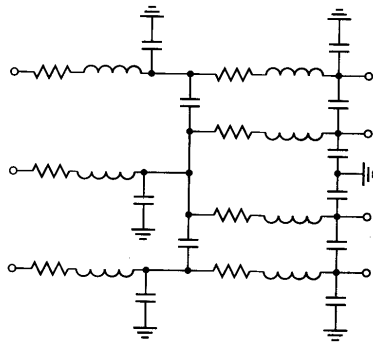


Capacitance-only model

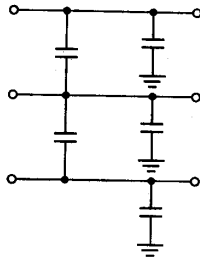
□ Parasitic wire models

- The lumped parameter modeling of resistive, capacitive and inductive effects on interconnect are distributed over entire wire length.
- This is necessary when wire length becomes much greater than its line width, $L_{wire} \gg W_{wire}$.
- We have effects due to the relationship of the wire to ground, and also between wires at different layers in the circuit geometry.
- We end up with “coupling” effects in the layout that must be managed, that are not present in schematic model.
- These are complex models that, fortunately, we can simplify under certain conditions (see next slide).

Wire Modeling-2



All-inclusive RLC model



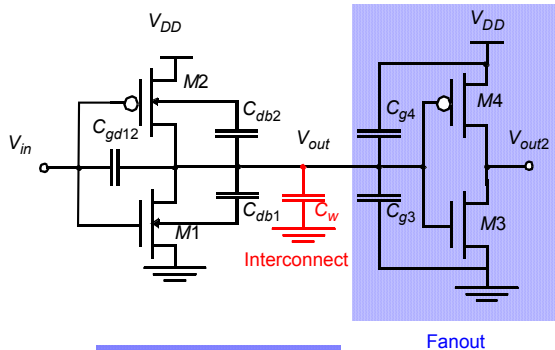
Capacitance-only model

Parasitic wire model simplification

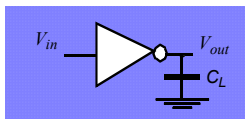
- Induction can be ignored if the wire resistance is large: $R_{\text{wire}} \gg L_{\text{wire}}$ for longer lines.
- A capacitance only model can be used IF (1) wires are relatively short, (2) wire cross section ($W_{\text{wire}} \times H_{\text{wire}}$) is large, OR (3) we use a low-resistivity interconnect material.
- A simplified capacitance model consisting only of wire-to-ground capacitance (ignoring inter-wire effects) can be used IF: (1) inter-wire separation is large, OR (2) wires run together in material for short distance.
- The specific values for when we use these model assumptions are to be derived by authors in the text.

Capacitance of Wire Interconnect

Capacitance wire model simplification (redux)



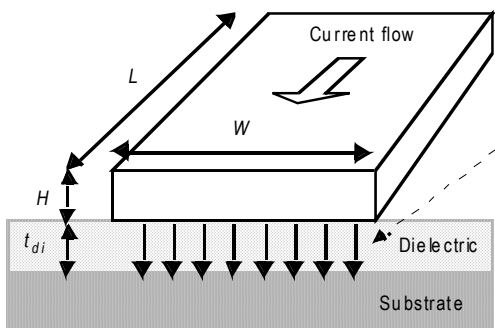
Simplified Model



- In the figure, we see how we incorporate the capacitance wire assumption into the schematic view.
- We have a “transmitter” (an inverter, with its device capacitances identified) connected to an output line that drives a *fanout* “receiver” load consisting of the transistors of another inverter.
- We can model this as the inverter transmitter (or driver) coupled to a load consisting of a capacitance, C_L , with voltages V_{in} and V_{out} .
- There is a relationship between C_L , C_{wire} and the load values on the *fanout* that is to be developed.

Capacitance - the Parallel Plate Model

□ Rectangular wire geometry

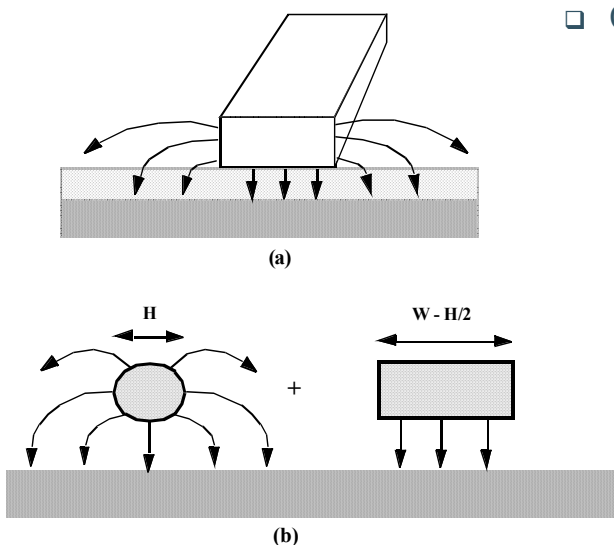


$$C_{int} = \frac{\epsilon_{di}}{t_{di}} WL$$

$$S_{C_{wire}} = \frac{S}{S \cdot S_L} = \frac{1}{S_L}$$

- We can adopt a “parallel-plate” capacitor model IF wire width is much greater than dielectric thickness: $W_{wire} \gg t_{di}$
- To minimize the effect of resistance as we scale the wire, we must keep cross section ($W_{wire} \times H_{wire}$) large.
- Smaller line widths, W_{wire} , allow more dense packing of circuits onto geometry (at cross-purposes).
- The (W_{wire} / H_{wire}) ratio: as it drops below unity, we must incorporate the “fringing” component of the capacitance model along with the “parallel-plate” component to obtain parameter C_{wire} .
- Capacitance is proportional to overlap between conductors, inversely proportional to their separation.

Capacitance – Fringing Field Model



□ Cylindrical wire geometry

- We simplify the fringing field geometry by assuming we have a cylindrical wire of diameter equal to wire thickness H_{wire} (compare with figure for parallel plate geometry).
- We assume parameter, w , the *per-unit-length wire width*, as follows: $w = W - H/2$. The per-unit-length parameter here is given as a function of total lumped-wire width and height. (See footnote, p. 139).
- **ERRATA:** Note the revised formula (equ. 4.2, p. 141) & modify in text!

$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\epsilon_{di}}{t_{di}} + \frac{2\pi\epsilon_{di}}{\log(2t_{di}/H + 1)}$$

Typical Permittivity Values

The values shown here are normalized relative to permittivity of free space, which is $\epsilon_0 = 8.854 \times 10^{-12} \text{ F/m}$.

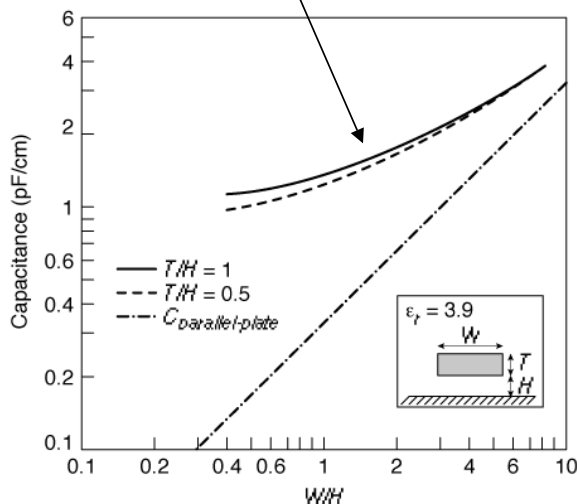
Insulators that are Starting to be used Due to lower Permittivity (and thus Lower C_{wire}).

Insulator most prominently in use today.

Material	ϵ_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide SiO_2	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Capacitance - Fringing versus Parallel Plate

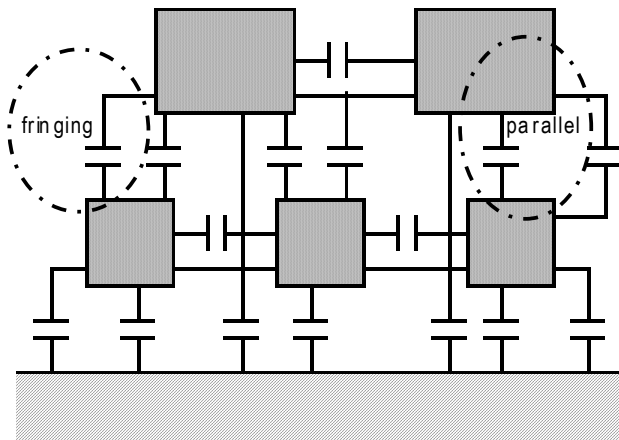
Plotting capacitance against the W/H ratio, with different values for the ratio between H/t_{di} .



□ The Modeling Continuum

- Looking at c_{wire} as a function of (W/t_{di}) , derived from $(W_{\text{wire}} / H_{\text{wire}})$ ratio.
- For larger values of $(W_{\text{wire}} / H_{\text{wire}})$, the c_{wire} approaches that of C_{pp} .
- For smaller $(W_{\text{wire}} / H_{\text{wire}})$ values, less than 1.5, closer to unity, C_{fringe} becomes more dominant component.
- Fringing capacitance can increase overall c_{wire} by > 10X for small W_{wire} values.
- Also, c_{wire} converges to a constant value ($\cong 1 \text{ pF/cm}$) if $W_{\text{wire}} < t_{\text{di}}$, i.e., capacitance is no longer a function of interconnect line width.

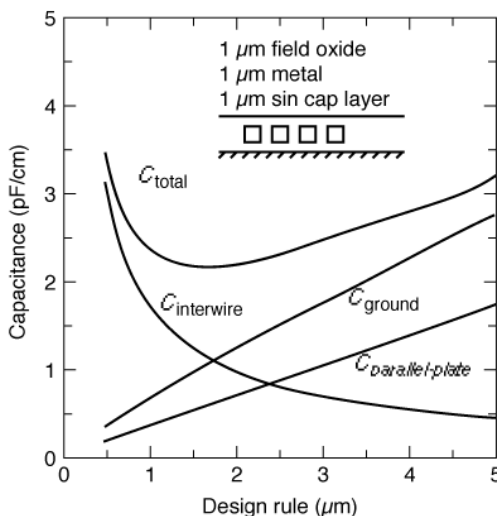
The Inter-wire Capacitance Model



- The Wire “micro-stripline” versus the wire interconnect hierarchy:
 - With only 1-2 layers of metal interconnect on top of the poly and diffusion, we can assume the additive capacitance model for parallel plate and fringe relative to ground.
 - Actual CMOS processes have many more layers, densely packed.
 - Each wire is coupled to ground substrate, and to neighboring wires on same and adjacent layers.
 - These “floating” capacitances have parallel plate and fringe aspects relative to time varying voltage levels of these other wire signal paths—a source of “crosstalk” noise.

Impact of Inter-wire Capacitance

- The bottom line:



(from [Bakoglu89])

- Inter-wire capacitances become dominant in multilayer interconnect structures.
- Effect is more pronounced at higher layers (further away from the substrate).
- Contribution of $C_{interwire}$: for parallel wires routed above a ground plane, with constant dielectric (t_{di}) and wire thickness (H_{wire}), while other dimensions (W_{wire} , T_{wire}) scaled .
- As $(W_{wire} / H_{wire}) < 1.75$, inter-wire effect dominates (as seen in the plot of Capacitance vs Line width).
- The figure in the plot “legend” shows the configuration assumption for this conclusion.
- Compare this result with slide #12 for C_{fringe} vs C_{pp} .

Wiring Capacitances ($0.25 \mu\text{m}$) – for examples

Table rows are capacitor's "top plate."
Table columns are its "bottom plate".

Use the Field values for C terms when placing wires over thick field oxide (SiO_2) that isolates different transistors.

C_{pp} values in upper row.
 C_{fringe} values in lower, shaded row.

Process supports 1 layer Poly and 5 layers Metal.

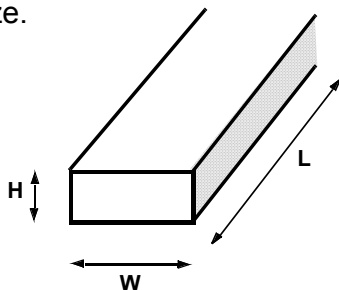
First 4 metal layers Use same H and t_{di} .
But 5th layer has $H_{m5} = 2H_m$ and $\epsilon_{di5} > \epsilon_{di}$.

	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88						
	54						
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

Wire Resistance Model

□ The bottom line:

- Resistance of a wire \propto wire length, and $1/\propto$ to cross section area ($H \times W$).
- Assume same rectangular geometry as for capacitance model.
- The "resistivity", ρ , of the wire material (expressed in Ohm-m) is a constant.
- The wire thickness, H , is also a constant (for a given technology), and can be expressed in terms of "sheet resistance" (expressed in "Ohms-per-square").
- Result is that R of a square wire segment is independent of its absolute size.



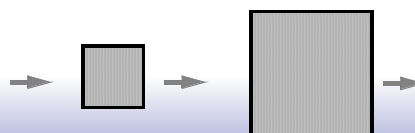
$$R = \frac{\rho L}{HW}$$

Cross-section area

Sheet Resistance

R_0 ← This should be R/L .

$$R_1 \equiv R_2$$



Interconnect Resistance

Material	ρ ($\Omega\text{-m}$)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

□ Resistivity ρ :

- Aluminum most often used for Metal interconnect material (low cost and process compatibility).
- Copper has better resistivity constant, however, and is finding its way into more prominent use in newer processes.

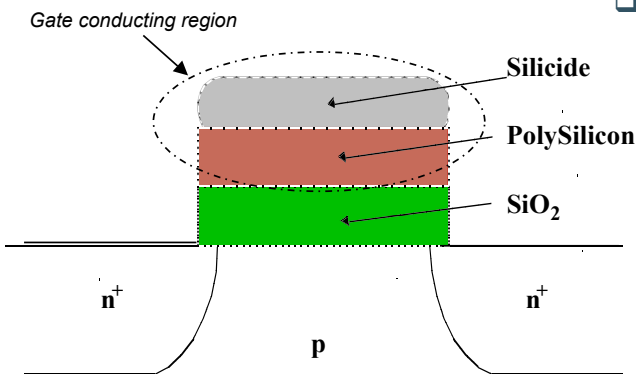
□ Sheet resistance R_{\square} :

Material	Sheet Resistance (Ω/\square)
n- or p-well diffusion	1000 – 1500
n^+ , p^+ diffusion	50 – 150
n^+ , p^+ diffusion with silicide	3 – 5
n^+ , p^+ polysilicon	150 – 200
n^+ , p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

- For the 0.25 micron process, we have avg. values for interconnect materials.
- This shows use of Diffusion, Poly and Metal lines as wires.
- Note use of a “Silicide” compound enables processing of Diff and Poly layers at high temp. to increase region’s conductivity.

Use of Polycide increases conductivity by reducing sheet resistance.

Interconnect – the Polycide Gate



□ Design Objective:

- Want to be able to use Poly and Diffusion materials as better conductors of current.
- Reduce resistance of conducting materials, Poly and Diffusion layers.
- Add a silicon compound layer on the gate Poly, source and drain Diffusion regions.
- Increases conductivity by reducing R_{\square} .

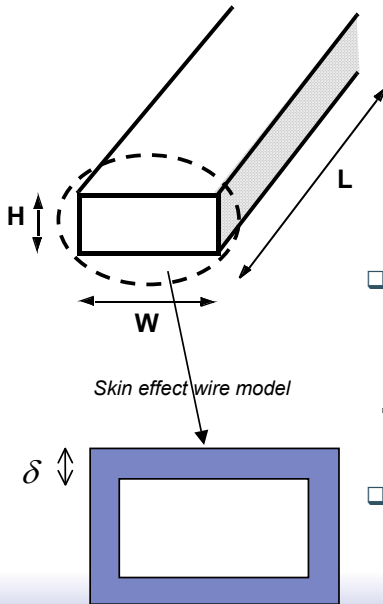
Silicides: WSi_2 , TiSi_2 , PtSi_2 and TaSi

Conductivity: 8-10 times better than Poly alone.

Resistance – Skin Effect

Resistance at very-high switching frequencies, in wider wires

- R is no longer linear, but is frequency dependent (GHz range, e.g., Pentium® clock frequency)
- Current flows nearer to surface of conducting wire, drops off beyond depth δ . Equ. 4.6
- Skin depth δ : depth at which current falls off to a value of e^{-1} of its nominal value.
 - Al at 1 GHz frequency, $\delta = 2.6$ microns.



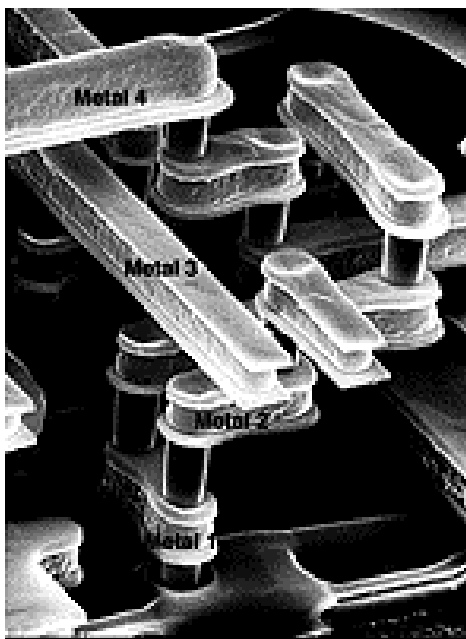
Skin effect approximation

- Assume uniform current flow in "outer shell" of rectangular wire with thickness of δ . Wire cross-section ($H \times W$) $\approx 2(W \times H) \times \delta$.
- Calculating r (i.e., R per unit length): Equ. 4.7

Implications

- Find the frequency f_s where $\delta = \frac{1}{2} \max(W, H)$. If $f > f_s$, then we'll have increased resistance. Eq 4.8
- Clocking: wide wires & high freq \Rightarrow "skin" r .

Minimizing Resistance



Employ selective Technology Scaling

- Scale L and W , leave H and t_{di} alone (as with capacitance)?

Use Better Interconnect Materials

- Reduces average wire-length
- e.g. Copper, Silicides

More Interconnect Layers

- Reduces average wire-length.
- But add more wiring layers, which increases capacitance effects (design tradeoff here).
- However, to minimize *contact resistance*, we want to keep signal wires on a single layer, and avoid excessive contacts and vias.

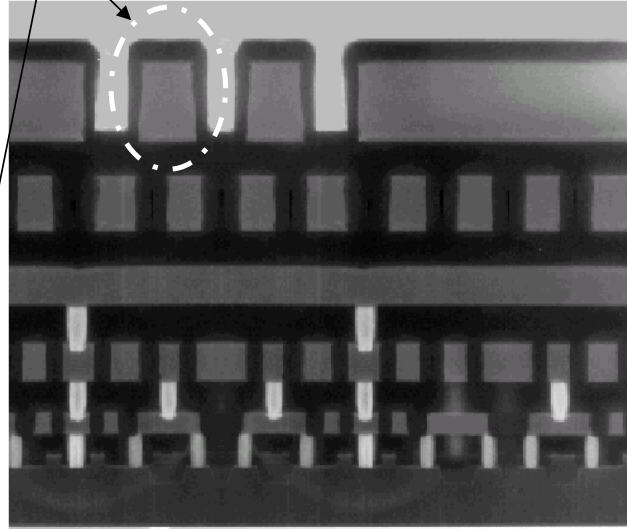
Example: Intel 0.25 micron Process

As we get to higher layers of metalization, we see W and H get much larger. This starts to change the model for resistance, and introduces inductance, in designs operating at higher switching frequencies (GHz range).

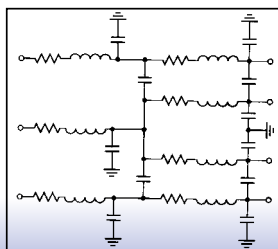
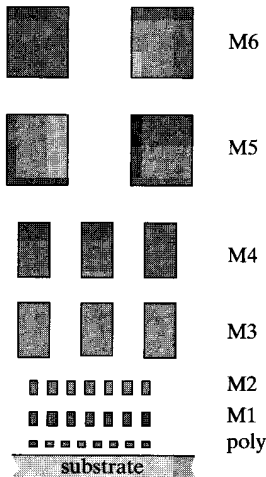
5 metal layers
Ti/Al - Cu/Ti/TiN
Polysilicon dielectric

LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	μm	μm	

Layer pitch, thickness and aspect ratio



Wire Inductance Model



□ Inductance effects – when?

Global

- Low resistive materials and wider wires at higher metal layers.
- Very high frequency switching.

□ Analysis method

intermodule

- Rather than compute wire inductance from geometry, use a *per-unit-length* relation between capacitance c & inductance l . Eq 4.10

Intercell

Intracell

- Assume approximate uniformity in surrounding insulator material.
- Insulator material properties define the relationship: *permittivity, permeability*.

□ Line impedance (Z)

- Inductance and resistance components.
- Want the frequency at which inductance component of Z becomes equal in value to resistive component (*per-unit-length*).

Continuum of Wire Models

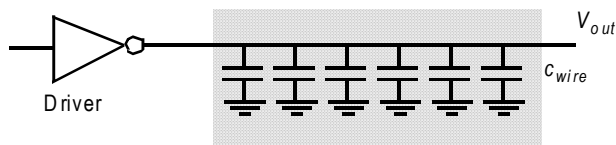
Wire Model Type	1. Ideal Wire	2. Lumped – C Dominant	3. Lumped - RC	4. Distributed rc Line (per-unit-length)	5. Lossy/less Transmission Line
Model Properties	-Simple line with no parasitics. -Same voltage present at all wire segments.	-Circuit parasitics distributed along wire length are lumped when C dominates, or interaction of R and C is small. -Lump as single C	-Circuit parasitics lumped at nodes along wire length. -Reduce transient wire behavior to RC network. -Use Elmore delay for RC tree. -Use 1 st order FX.	-Distributed <i>rc</i> wire model. -Signal moves through wire via diffusion-Eq 4.18 -Voltage at node <i>i</i> solved via partial diff. equ. -Diffusion equ.	-Distributed <i>rlc</i> wire model. -Signal moves through wire as wave (<i>c</i> to <i>l</i> to <i>c</i>). -Lossless: no <i>r</i> . -Lossy: <i>r</i> effects.
When Model is Used	-Early in the design process, when focusing on properties and behavior of the transistors. -Model gate wires	-When R values are small w/r/t C. -When operating at lower switching frequencies. -Use it to model wire loads.	<i>Use to model interconnect when studying the supply distribution network.</i>	-When goal is to minimize long line delay and signal degradation. -Approximated by using RC-ladder network.	- When switching speeds become fast, wire material with low R, but inductance starts to dominate delay behavior.
Limitations of Model	- Doesn't take real properties of interconnect into account.	-Wire still has equal voltage present along all wire segments. -Wire doesn't introduce delay. -Not useful for analyzing V_{xx}	- Lumped RC assumption inaccurate for long wires (number of N segments grows large).	-Distributed <i>rc</i> is complex and has no closed-form solution, only approximations. -Generally use the RC ladder configuration.	-Lossless useful for PCB wires. -Lossy required for on-chip wires, - Simplifies down to distributed <i>rc</i> line (model 4).

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Devices

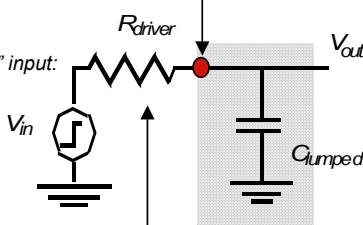
The Lumped Model (Dominant C)



We use Kirchoff's current equation at the node to form the differential equation.

$$(V_{out} - V_{in}) / R_{driver} + C_{lumped} dV_{out}/dt = 0$$

Applying a "step" input:



Reducing source R_{driver} resistance is a major design concern. See example 4.5, p152.

□ Model axioms

- Single parasitic component is dominant, in that R is small relative to C (large area, better materials) .
- Lump capacitance into a single circuit element.

□ Model topology

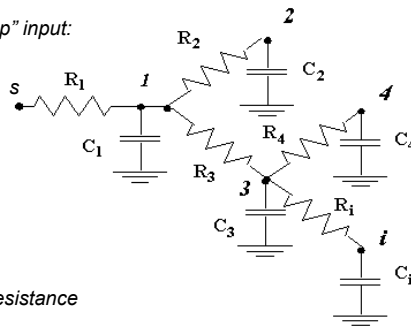
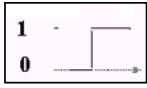
- Driver is modeled as voltage source with source resistance.
- Load is modeled as capacitor at the end of the wire.

□ Differential equation

- Kirchoff's current equation, replacing I for capacitance and Ohm's law components.
- Assuming step input, we know form of transient ($1 - e^{-t/RC}$) for the network time constant.

The Lumped RC Model

Applying a "step" input:



Shared path resistance

$$R_{ik} = \sum R_j \Rightarrow (R_j \in [\text{path}(s \rightarrow i) \cap \text{path}(s \rightarrow k)])$$

$$\tau_{Di} = \sum_{k=1}^N C_k R_{ik}$$

Model axioms

- Lump total wire resistance of each wire segment into single R between nodes in network.
- Lump total capacitance into single node capacitor to GND.
- Single differential equ., single RC time constant for solution.

Model topology

- RC tree: (1) single input node, (2) C_i between node i and GND, (3) no resistive loops.
- Unique resistive path from source node s to any node i .

Elmore delay calculation

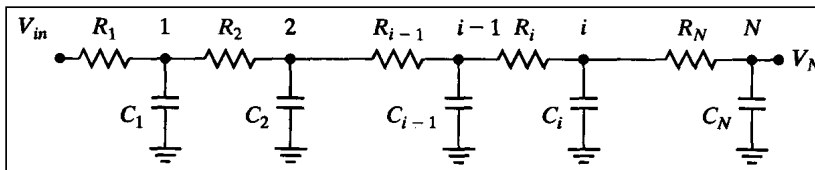
- Path resistance, R_{ij} .
- Shared path resistance: s to k , i .
- Elmore delay at node i : Equ 4.13

Lumped RC Model - Elmore Delay

Consider the simple, non-branched RC ladder network: a good approximation of an R-C wire. Using 4.13, we reach a simplification where the shared-path resistance is replaced by the path resistance. This is summed with capacitance at each node over the wire segments.

A wire of length L is partitioned into N identical segments, each with length L/N . Capacitance = cL/N , Resistance = rL/N (these are per-unit-length for each segment).

Using Elmore, we compute the dominant time constant of the wire.



$$\tau_{Di} = \sum_{k=1}^N C_k R_{ik}$$

This reformulation of Equ. 4.13 into 4.14 (p. 154) allows the RC tree to be represented (approximately) by the RC ladder network.

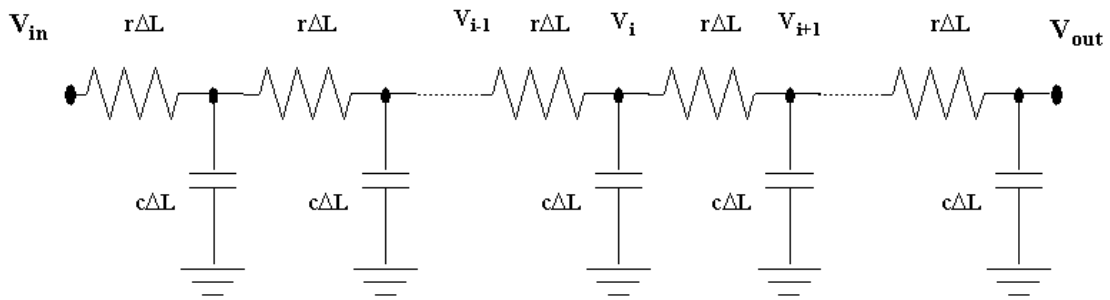
Time constant τ_i can be derived for any node i in the network:

$$\tau_{Di} = C_1 R_1 + C_2 (R_1 + R_2) + \dots + C_i (R_1 + R_2 + \dots + R_i)$$

$$\tau_{DN} = \sum_{i=1}^N C_i \sum_{j=1}^i R_j = \sum_{i=1}^N C_i R_{ii}$$

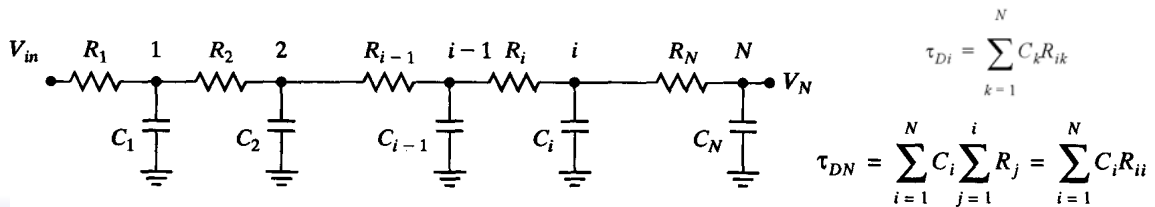


The Elmore Delay Model - RC Chain



Consider the simple, non-branched RC ladder network: a good approximation of an R-C wire. Using 4.13, we reach A simplification where the shared-path resistance is replaced by the path resistance.

A wire of length L is partitioned into N identical segments, each with length L/N . Capacitance = cL/N , Resistance = rL/N (these are per-unit-length for each segment). Using Elmore, we compute the dominant time constant of the wire.



Lumped RC Model – Dominant Time Constant

Assume: Wire modeled by N equal-length segments

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \dots + Nrc) = (rcL^2) \frac{N(N+1)}{2N^2} = RC \frac{N+1}{2N}$$

We can compute the dominant time constant $\tau = RC$ of the wire by summing over N segments, extracting the Length components L/N for both r and c (per-unit-length) multiplied by the series expansion. Reformulating terms, and inserting $R = rL$ and $C = cL$ as total lumped R and C of the wire.

For large values of N – the $(N+1)/2N$ goes to $1/2$:

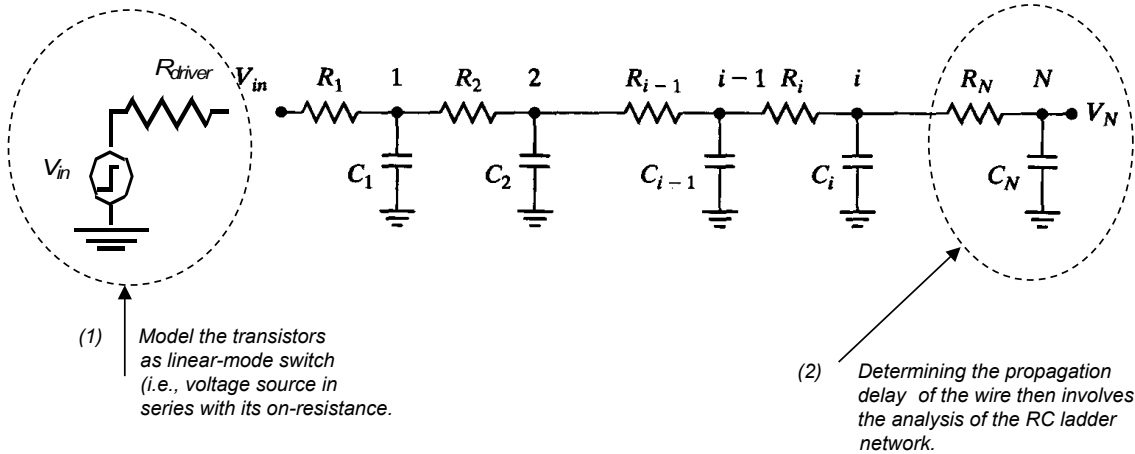
$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

As N grows large, the lumped RC model approaches that of the distributed rc line model, with conclusions:

- (1) Delay of a wire is quadratic function of wire length L . (So, doubling wire length quadruples line delay.)
- (2) Delay predicted using lumped RC model is approximately half as accurate (in terms of delay calculation) as the distributed rc line model.
- (3) The Elmore delay calculation only considers the dominant time constant, ignoring the others that would be associated with other RC terms, so the delay associated with the dominant RC is crude, depending on wire length.

Lumped RC Model – Plugging It In

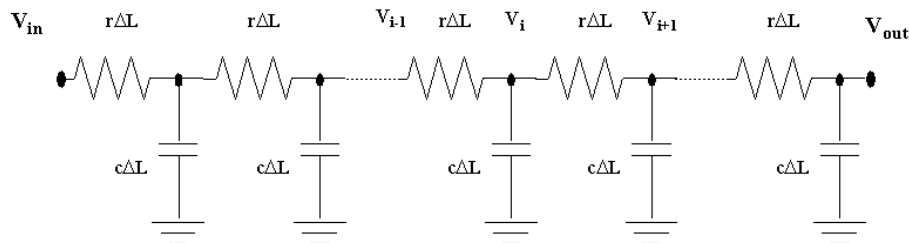
We can now relate the wire model to the transistor model as follows:



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Distributed rc Model

Lumped RC model is “pessimistic” in its assumption, so we increase the accuracy by distributing the resistance and capacitance throughout wire segments (r and c defined per-unit-length).

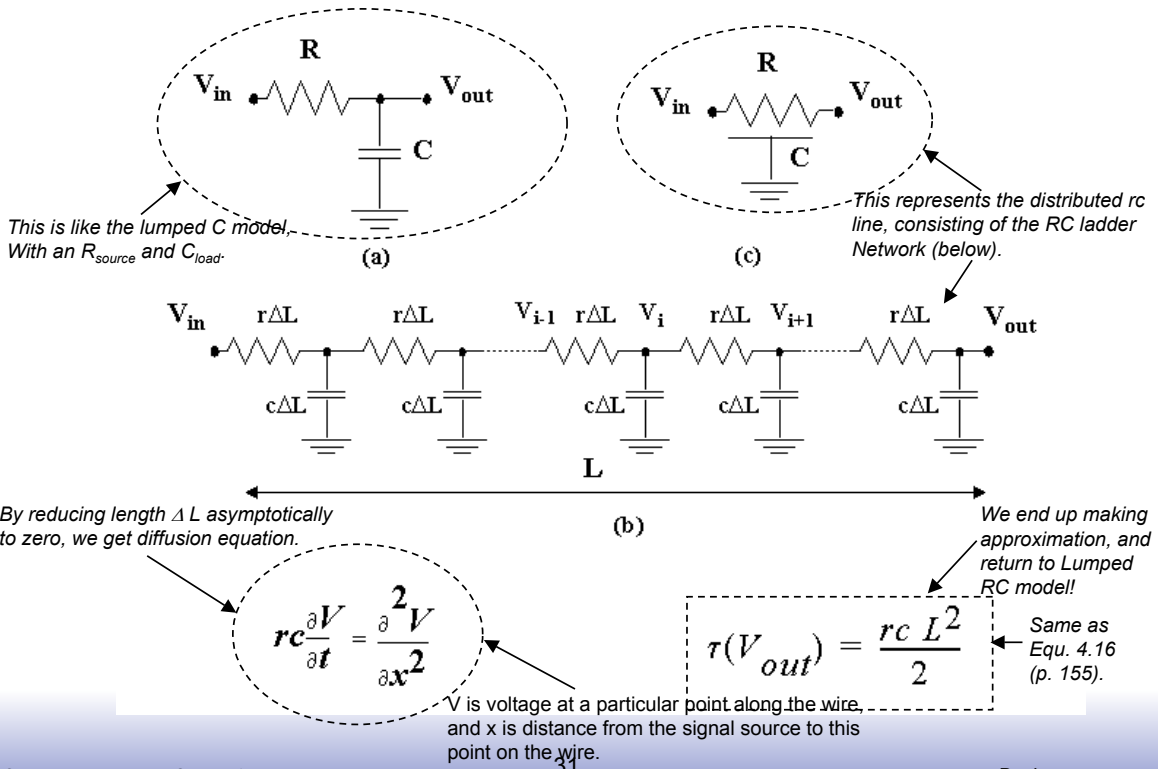


A wire of length L is partitioned into N identical segments, each with length L/N . Capacitance = cL/N , Resistance = rL/N (these are per-unit-length for each segment).

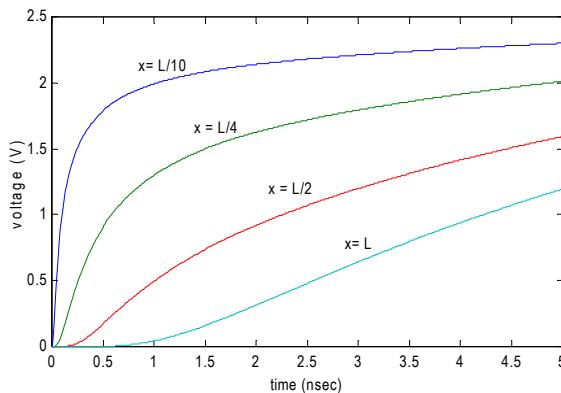
Using Elmore, we compute the dominant time constant of the wire.

The voltage at a given node can be solved using partial differential equations (Equ. 4.17 -> Equ. 4.18).

The Distributed RC-line



Step-response of RC Wire Model



Basic point from the graph: shorter lines have better response than longer ones. Longer lines take longer to reach their driven value, which means the delay of the line affects how long it takes for the signal strength to reach the driven level (here transitioning logic 0 to 1).

Behavior assumption

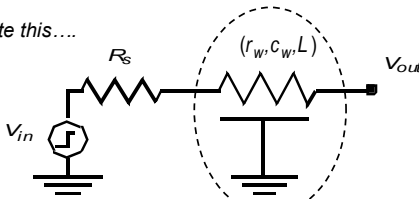
- We reduce the per-unit-length, ΔL , asymptotically to zero
- Lump total capacitance into single node capacitor to GND.
- Single differential equ., single RC time constant for solution.

Plot meaning

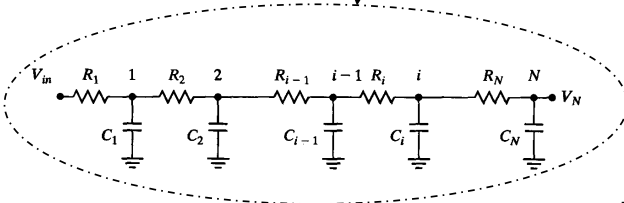
- Response of the rc-wire to an input step function (0 → 1).
- V is voltage at a particular point along the wire, and x is distance from the signal source to this point on the wire.
- We see the signal rise times of the unit step response in the distributed rc network, given different line lengths, L .

Reduction in Distributed rc Model

Formulate this....



Like this....



To get this....

$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

$$t_p = 0.69 R_s C_w + 0.38 R_w C_w$$

Behavior assumption

- We have rc-line of length L (not inductance L), driven by voltage source with series resistance R_s representing the driving gate.
- Apply Elmore's formula to obtain approximation of t_p , the total propagation delay from the time constant terms for the network.
- As before $R_w = rL$ and $C_w = cL$ (again, L is wire length).

Delay calculation

- Solve for time constant τ_D in terms of Elmore tree derivation of resistive-capacitive wire (p. 155).
- The delay introduced by wire resistance becomes dominant when: $(R_w C_w)/2 \geq R_s C_w$ or when: $L \geq 2R_s/r$.

Distributed rc Line - Heuristics

Under different conditions, we can reduce the complexity of the distributed rc model to either the Lumped C, or Lumped RC models.

The factor that governs this model selection is the relationship between propagation delays of the driving gates and that of the line itself.

However, we can look at the line length to give us some guidance (defined by a critical length, L_{crit}).

- rc delays should only be considered when $t_{pRC} \gg t_{pgate}$ of the driving gate.

$$L_{crit} \gg \sqrt{t_{pgate}/0.38rc}$$

Rc delay becomes dominant for interconnect wires longer than L_{crit} . Therefore, we use the Lumped RC model.

- rc delays should only be considered when the rise (fall) time at the line input is smaller than RC, the rise (fall) time of the line.

$$t_{rise} < RC$$

- when not met, the change in the signal is slower than the propagation delay of the wire.
 - Therefore, we use Lumped C model in this case.

Analysis Examples (Rabaey text)

- Example 4.1, p. 144.
 - Capacitance of metal wire
 - Factor of 2x for C_{fringe} calculation due to both sides of wire cylinder “fringing”.
 - Uses Table 4-2, p. 143, and Table 4-3, p. 144.
- Example 4.2, pp. 146-147.
 - Computing total resistance from R_{\square} .
 - Comparing resistance of metal vs. Poly lines.
- Examples 4.3, p. 148.
 - Resistive skin effect analysis.
 - Plotting skin effect to determine at what line widths it becomes noticeable.
- Example 4.4, p. 150.
 - Inductance of metal wires of different widths.
 - Calculate $c_{pp} + c_{fringe}$ (also using 2x factor for c_{fringe} from Ex 4.1).
 - Identifying at what operating frequency and given wire widths we start to see inductance effects.
- Example 4.5, p. 152.
 - Lumped capacitance of wire, using Kirchoff's law, Ohm's law, RC time constant.
- Examples 4.6, p. 154. & 4.7, p. 155
 - Elmore calculation of RC-induced wire delay of tree-structured network.
- Examples 4.8, 4.9
 - Distributed rc line calculations that reduce to Lumped RC (Elmore) and Lumped C

Summary

- **The continuum of wire modeling.**
 - **We looked at different models and how they address the issue of propagation delay through the interconnect network.**
 - **We used various techniques, based on formulating the RC time constant, given a step input (transition from logic 0 to logic 1) from the gate “driver” of the line and “load” on the other end.**
- **Modeling continuum: (1) wire model, (2) lumped parameter models (C-alone, RC), (3) distributed rc line model, (4) transmission line model (lossless, lossy).**
 - **These models progress from simple to complex, their use depending on the effects being studied and the accuracy required.**
 - **Different automated tools may support some set of these assumptions in the analysis capabilities provided to the designer.**
- **Examples from Ch4 text – the progression of modeling results for the .25 micron CMOS process.**