

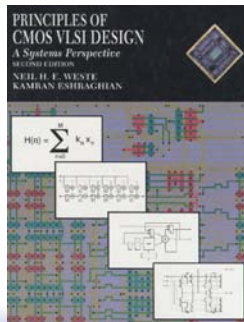


# CSCE 613 – Week 5 Fall 2005

Introduction to CMOS VLSI Design

## CMOS Transistor Layout

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### Topics of Week 5

- Discuss the layout of CMOS transistors to form various circuit structures according to design rules (materials from Chapters 5 & 6 of Weste et al., © 1994 Addison Wesley Publishers, Inc.).
- We discuss a collection of design rules governing the placement of transistors and their interconnect in tightly-defined rules, based on the  $\lambda$  proportional constant. However, we use *stylized layouts*, omitting certain details.
- We look at constructing examples of logic elements, including NOT, NAND, NOR gates (on which most CMOS logic circuits are built). We'll see that there are many possible ways to layout a specific logic circuit, depending on the design objective, and in keeping with the design rules.
- We also look at restrictions in circuit layout when given a partially implemented structure in the silicon substrate—the Sea of Gates (SOG examples of ASIC layout technology).

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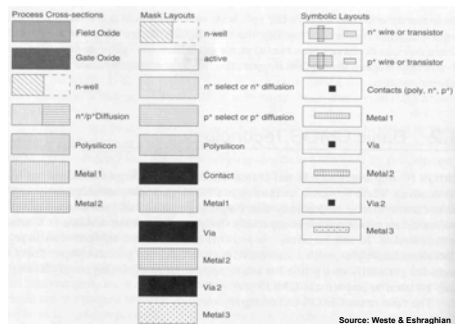
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### CMOS Process Layout & Cross Sections



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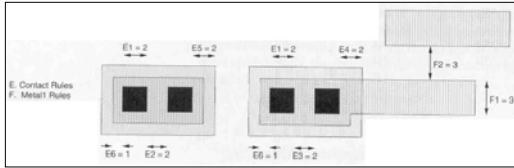
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## Design Rules – Metal1

	$\lambda$ RULE	$\lambda/\mu$ RULE (0.5 $\mu$ )	$\mu$ RULE
<b>F. Metal1</b>			
F.1 Minimum size	$3\lambda$	1.5 $\mu$	1 $\mu$
F.2 Minimum spacing	$3\lambda$	1.5 $\mu$	1 $\mu$



Source: Weste & Eshraghian

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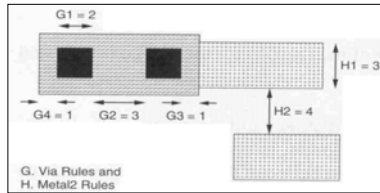
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## Design Rules – Via

	$\lambda$ RULE	$\lambda/\mu$ RULE (0.5 $\mu$ )	$\mu$ RULE
<b>G. Via</b>			
G.1 Minimum size	$2\lambda$	1 $\mu$	0.75 $\mu$
G.2 Minimum spacing	$3\lambda$	1.5 $\mu$	1.5 $\mu$
G.3 Minimum Metal1 overlap	1 $\lambda$	0.5 $\mu$	0.5 $\mu$
G.4 Minimum Metal2 overlap	1 $\lambda$	0.5 $\mu$	0.5 $\mu$



Source: Weste & Eshraghian

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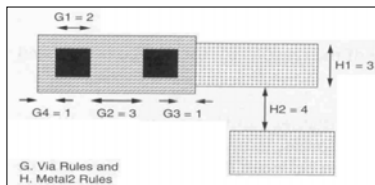
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## Design Rules – Metal2

	$\lambda$ RULE	$\lambda/\mu$ RULE (0.5 $\mu$ )	$\mu$ RULE
<b>H. Metal2</b>			
H.1 Minimum size	$3\lambda$	1.5 $\mu$	1 $\mu$
H.2 Minimum spacing	$4\lambda$	2 $\mu$	1 $\mu$



Source: Weste & Eshraghian

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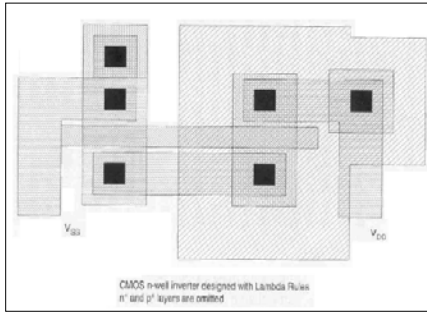
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### Example - CMOS n-well Inverter



Source: Weste & Eshraghian

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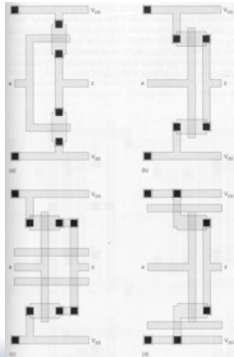
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### The CMOS Inverter – Layout-1



#### □ Design alternatives

- Topology variations may be used to enable non-planar connections between different structures.
- Version (a) is the basic inverter layout, derived directly from the schematic.
- Version (b) has the transistors aligned horizontally rather than vertically.
- Version (c) has two metal lines that are routed through the region of the inverter, and the common drain connection is made using Metal2 or Poly.
- Version (d) has metal lines running at top and bottom, wherein the connections to power and ground are made in the diffusion layer.

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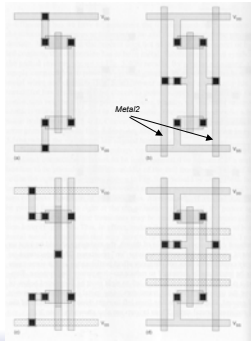
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### The CMOS Inverter – Layout-2



#### □ Design alternatives

- Here, we add a 2<sup>nd</sup> layer of Metal interconnect, which may be used to run  $V_{DD}$  and  $V_{SS}$ .
- Alternately, the Metal layer may be used to strap Poly in a parallel connection, to reduce long poly runs.
- Versions (a) and (b) here show possible minor variations from previous versions, except Metal2 with Metal1 to Metal2 connections.
- Versions (c) and (d) show more strict routing of lines (vertical Poly, Metal2, and horizontal Metal1, Metal3). In this case, Metal3 is used for power and ground connections.

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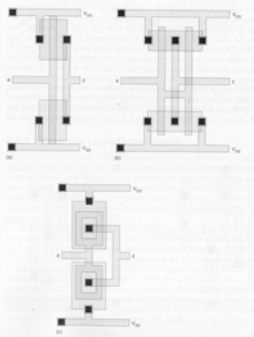
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## The CMOS Inverter – Layout-3



### □ Design alternatives

- Version (a) has increased size of the transistors to increase the drive capability.
- Alternately, Version (b) shows a large driving inverter comprised of multiple inverters connected in parallel. Note the transistors are placed "back to back" (a common configuration) to minimize drain capacitance, thus affecting drive gain.
- Version (c) shows a transistor configuration where a round transistor ("donut") is created to reduce drain capacitance, thereby increasing the transistor gain.

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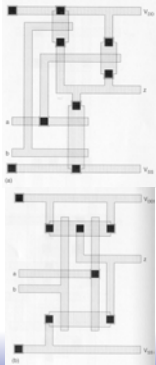
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## The CMOS NAND – Layout



### □ Design alternatives

- Version (a) is a direct conversion of the schematic.
- Version (b) orients the transistors horizontally and the Polysilicon gate signals vertically.
- Note also in (b), the placement of transistors back-to-back, and the common source and drain connections on the n- and p-channel transistors.
- Note also how you can tell the series connections of transistors versus the parallel connections.

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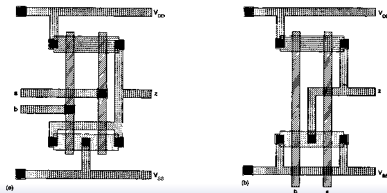
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## The CMOS NOR – Layout

### □ Design alternatives

- Version (a) is, again, based on direct mapping of the schematic.
- Version (b) uses another trick, has less drain area connected to the output of the NOR gate. This results in a faster gate.




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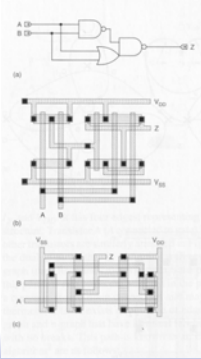
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## The CMOS XNOR – Layout



### □ Design layout scheme

- Transistors are grouped in strips to allow maximum source/drain connection by abutment. To achieve better grouping, Poly columns are allowed to interchange to increase abutment.
- Resultant groups are placed in rows with groups maximally connected to VSS and VDD rails placed toward these signals. Row placement is then based on the density of other connections.
- Routing is achieved by vertical Diffusion or "Manhattan" (horizontal and vertical) metal routing.

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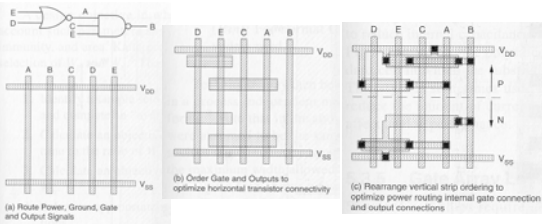
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## CMOS Logic Function – Layout




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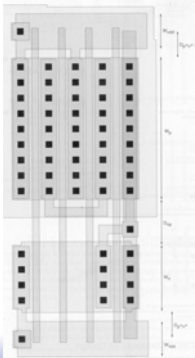
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## A CMOS Standard Cell



### □ Cell design

- When designing standard cells, geometric regularity is required, while maintaining common electrical properties.
- Goal is to fix the physical height of cell, while varying width according to function.
- The n-transistors have height  $W_n$ , p-transistors have height  $W_p$ , separated by distance  $D_{np}$  (rule-driven separation between active areas).
- Power ( $V_{DD}$ ) and ground ( $V_{SS}$ ) buses run along top and bottom.
- Internal cell area used for routing transistors of specific gates.
- Properties for power dissipation, noise immunity, propagation delay relate to size ratio ( $W_p/W_n$ ).
- Most CMOS gates have ratios = 1, where  $W_p = W_n$ .

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