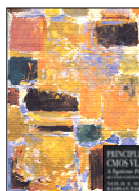
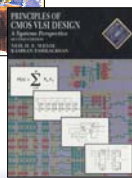




CSCE 613 – Week 4
Fall 2005
CMOS VLSI Design



Rabaey, Chandrakasan, and Nikolic, 2003.



Weste and Eshraghian, 1995.

CMOS Transistor Models

(part 2 – resistance, capacitance)

Adapted/extended by James P. Davis, Ph.D.
 Dept. of Computer Science & Engineering
 University of South Carolina

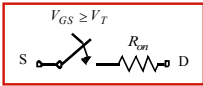
Topics of Week 4

- Discuss the CMOS transistor – a simpler “switch” model, but considering static and dynamic effects of resistance and capacitance.
- This material is from Chapter 3 – Rabaey et al., § 3.3.2 (second part), pp. 104-114. Slides for Chapter 3, #s 34-46. The Rabaey text is pretty good in this material, but I still augment with narrative from the Weste et al. text (© 1995 Addison Wesley, Inc.)
- The continuing focus is on different aspects of device modeling that are relevant to our set-up of building high-performance, low-power systems out of these devices. The analysis now progresses to look at Capacitance as a function of V_{GS} (moving from cut-off to linear) and V_{DS} (moving between linear and saturation).
- This material is important: (1) if you are going to be a VLSI device engineer, where you are designing the geometry of component structures in a new technology library accompanying a new process, and (2) if you are going to be a VLSI systems engineer and you are going to design high-speed, low-power circuits on some aggressive CMOS technology platform.

Summary of MOS Transistor Operating Regions

- Strong Inversion $V_{GS} > V_T$
 - Linear (Resistive) $V_{DS} < V_{DSAT}$
 - Saturated (Constant Current) $V_{DS} \geq V_{DSAT}$
- Weak Inversion (Sub-Threshold) $V_{GS} \leq V_T$
 - Exponential in V_{GS} with linear V_{DS} dependence

The Transistor as a Switch

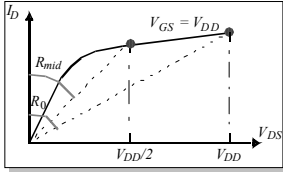


This model is even simpler than the Unified Model introduced in the last lecture.

Transistor switches between having an infinite "off" resistance, and having a finite "on" resistance.

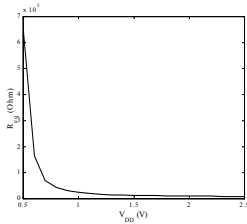
This resistance is affected by the dynamic behavior of the switching activity; we simplify it so that we assume an average resistance value of the endpoint of the operating region under consideration.

See example 3.8 Rabaey et al., pp. 104 – 105.



$$R_{av} = \frac{1}{2} \left(\frac{V_{DD}}{I_{Dsat}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{Dsat}(1 + \lambda V_{DD}/2)} \right) = \frac{3}{4} \frac{V_{DD}}{I_{Dsat}} \left(1 + \frac{5}{8} \lambda V_{DD} \right)$$

The Transistor as a Switch



Points of the model:
Resistance is inversely proportional to WL ratio; thus, doubling the width cuts resistance by ½.

For $V_{DD} \gg V_T + V_{DSAT}/2$, resistance becomes independent of supply voltage.

Once supply voltage approaches V_T , the resistance increases dramatically.

The simulation curve shows R_{eq} for 0.25 micron CMOS process as $f(V_{DD})$.
 $V_{GS} = V_{DD}$, $V_{DS} =$ from V_{DD} to $V_{DD}/2$.

Table 3.3 Equivalent resistance R_{eq} ($WL = 1$) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by WL .

V_{DD} (V)	1	1.5	2	2.5
NMOS ($\text{k}\Omega$)	35	19	15	13
PMOS ($\text{k}\Omega$)	115	55	38	31

Overview of MOS Model Components

□ Resistance Models

- Resistance calculations for conducting layers
 - Sheet resistance R_s for metal.
 - Sheet resistance for Polysilicon.
 - Resistance for Diffusion.
 - Resistance calculations for non-rectangular areas
- Resistance calculations R_c for Transistor-forming channel areas.
- Resistance calculations for Contacts and Vias.

□ Capacitance Models

- MOS Capacitor calculation 'Co' (without Source and Drain).
- Load Capacitance
 - Gate capacitance (of inputs connected to output of gate).
 - Diffusion Capacitance (drain regions connected to outputs).
 - Routing Capacitance (of connections between outputs and other inputs).

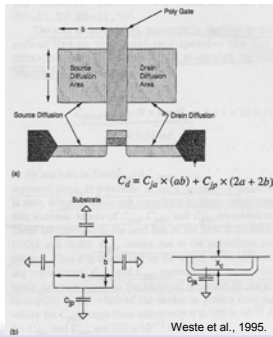
Diffusion Capacitance

Definition

- Shallow n+, p+ diffusions form source and drain terminals.
- Diffusion regions are used as wires.
- Diffusion regions have C to substrate or well, dependent on the V between diffusion and bulk (or well), and area of depletion region separating diffusion and bulk/well.

Behavior

- Cd is a function of diffusion to junction Area. Also a function of base area and sidewall area periphery.
- Sidewall capacitance assumes constant depth diffusion, and is periphery capacitance per unit length. Finite depth Xc.
- Cj: junction capacitance per Sq. (microns²).
- Cjw: periphery capacitance per depth (microns).
- a: width of diffusion (microns).
- b: length of diffusion (microns).



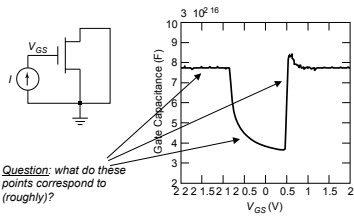
Simplifying the Diffusion Capacitance

Replace non-linear capacitance by large-signal equivalent linear capacitance which displaces equal charge over voltage swing of interest

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

Capacitances in 0.25 μm CMOS process



Question: what do these points correspond to (roughly)?

JD: This is a simulation plot of capacitance for minimum sized nMOS 0.25 micron technology.

The gate capacitance is measured in 10⁻¹⁶ Farads (the axis label is messed up in the figure).

	C _{ox} (fF/μm ²)	C ₀ (fF/μm)	C _j (fF/μm ²)	m _j	φ _b (V)	C _{jw} (fF/μm)	m _{jw}	φ _{top} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Week 4 Summary

- Circuit effects with CMOS transistors
 - Resistance.
 - Capacitance.
- We can assess the performance of the devices we design
 - Based on topology and geometry of our devices in the material substrate.
 - We attempt to design in such a way as to minimize these effects.
