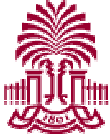

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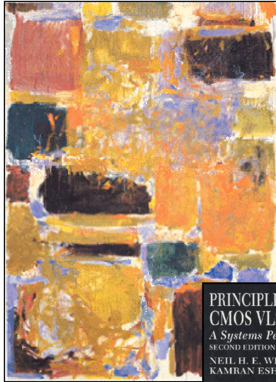
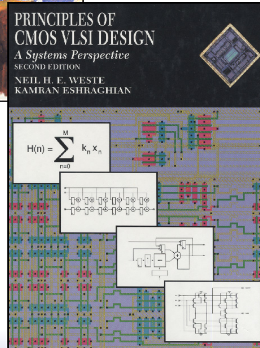


Rabaey, Chandrakasan, and Nikolic, 2003.



Weste and Eshraghian, 1995.

CSCE 613 – Week 3
Fall 2005

CMOS VLSI Design

CMOS Transistor Models

(part 1 – behaviors & parameters)

Adapted/extended by James P. Davis, Ph.D.
Dept. of Computer Science & Engineering
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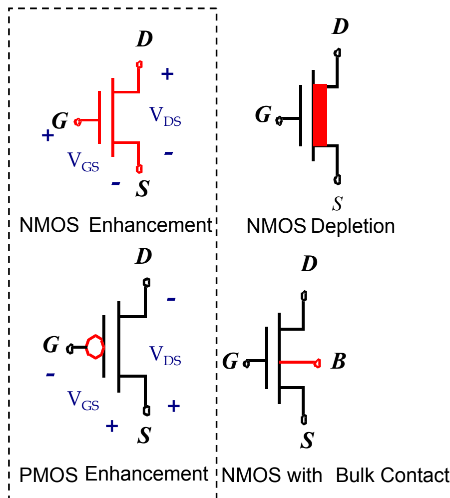
Topics of Week 3

- **Discuss the CMOS transistor – this time, we want to look at some of the modeling issues associated with MOS transistors. In a sense, we are elaborating on our basic understanding of the devices—but with a focus on issues that VLSI IC designers must contend with when changing technology due to device scaling.**
- **This material is from Chapter 3 – Rabaey et al., § 3.3.1, 3.3.2 (first part), pp. 87-106. Slides for Chapter 3, #s 20-36. In areas where the Rabaey text is lacking in clear explanation, I augment with narrative from the *Weste et al.* text (© 1995 Addison Wesley, Inc.)**
- **The focus is on 6-7 different aspects of device modeling that are relevant to our set-up of building high-performance, low-power systems out of these devices. The logic argument moves through the assigned reading.**
  - **However, I found the flow of this material very confusing and somewhat disorganized; it is not clear as to what is the authors' point in this presentation of material.**
  - **You actually don't get a glimpse of this until the last section of Ch3, so I will present this material in a reorganized fashion, with some references to Weste et al., when points need clarification.**

MOS Transistors - Types and Symbols



Note: current CMOS device transistors are "enhancement" mode only.

Ref: [Weste et al., 1995]

- The Digital Systems abstraction
  - A MOS transistor is an analog device for which we operate under conditions where we treat it as a digital device (e.g., DC operation).
- The MOS abstraction
  - A "majority carrier" device, the current in conducting channel (between drain and source) is controlled by voltage applied to gate.
  - nMOS – majority carrier is electrons, so a "+" voltage at the gate "enhances" number of electrons in channel, increasing conductivity.
  - pMOS – majority carriers are holes, so '-' voltage at gate "enhances" number of holes in channel, in creasing conductivity. *Ref: [Weste et al., 1995]*
- Enhancement versus Depletion mode
  - Difference between two modes has to do with whether there is a "bias" or voltage difference between the supply voltage, V_{DS}, and the control voltage, V_{GS}.
  - Enhancement mode devices conduct current, I_D, across the channel under the gate when a positive difference (nMOS) or negative difference (pMOS) exists between V_{DS} and V_{GS}. *Ref: [Weste et al., 1995]*
  - Depletion mode conducts I_D when $V_{DS} = V_{GS}$.

nMOS Transistor – Taxonomy of Scenarios

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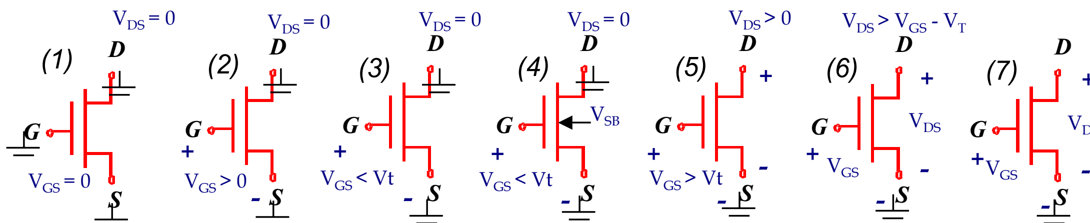
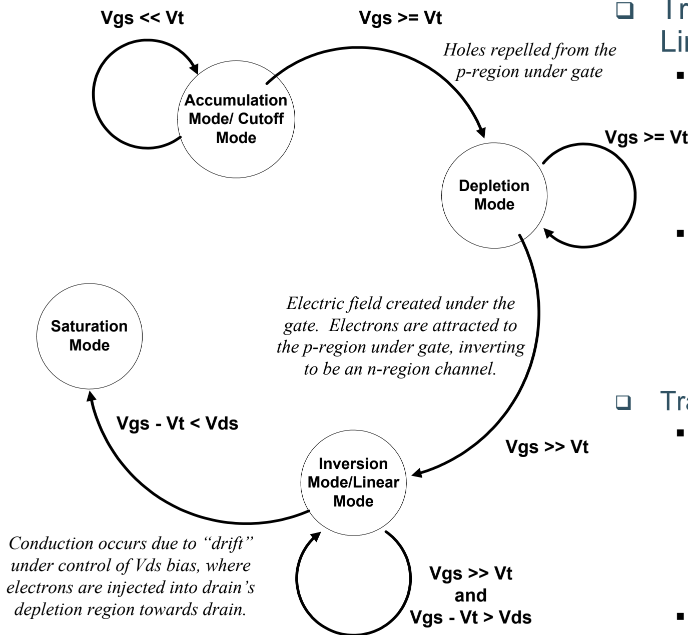


No gate bias voltage	Small gate bias voltage	Increased gate voltage	Body-bias in substrate	Resistive or linear mode	Saturation mode	Velocity saturation
MOS device is cutoff. High resistance is between drain and source terminals.	Gate and bulk substrate form plates of a capacitor with gate oxide under the gate as the dielectric. It acts like a pn-junction diode; charge is depleted between "plates".	Depletion surface "inverts" to n-type from p-type material. Further increase in V_{GS} has no further effect, but charge concentration in inversion layer increases.	We next look at the body-well bias in the substrate. The bias, V_{SB} is small, i.e. V_{SB} > -0.6v. Bias in the bulk essential to preserve diodes in well to substrate as "reverse-biased".	Voltage difference cause I_D current to flow, drain to source. The volts under channel is $V(x) > V_T$ for entire length of channel, $0 \leq x \leq L$.	Channel voltage not uniform, less than V_T. $V_{GS} - V(x) < V_T$. Conducting channel pinched off. Channel thickness is gradually reduced (from S to D) until pinch-off.	Increasing V_{DS} (although I_D is independent in saturation), causes E field change. Depletion region grows, shortening channel. Velocity saturation, $V_{DS} \Rightarrow V_{DSAT}$. Reduces amount of I_D transistor can deliver.

Transistor Abstract State Sequence



- Transitioning from Cut-off mode to Linear mode
  - We can illustrate this with a state diagram, showing how a gate bias voltage increase causes transitions in the underlying p-region to create a conducting channel between the n-wells in the nMOS transistor.
  - If the inversion under the gate (i.e., in the n-channel) is "weak", then the drain current, I_D, is dependent on the gate and drain voltages (V_{GS} and V_{DS}), and we are operating in "linear" or "resistive" mode.
- Transitioning from Linear to Saturation
  - If the n-channel region is "strongly inverted", as a result of $V_{DS} > V_{GS} – V_T$, and the potential $V_{GD} < V_T$ (the gate-to-drain voltage less than threshold). Channel is "pinched off", not reaching drain. Voltage across channel is $V_{GS} – V_T$, independent of V_{DS}.
  - Note how current I_D is dependent initially on both V_{GS} and V_{DS}, then only on V_{GS}. when in saturation mode. *Ref: [Weste et al., 1995]*

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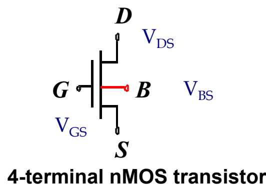
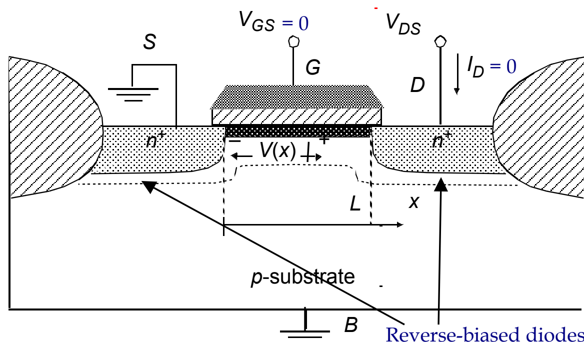
nMOS Transistor in Cutoff Mode



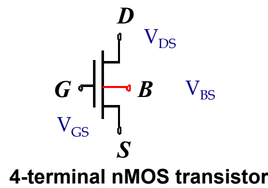
4-terminal nMOS transistor



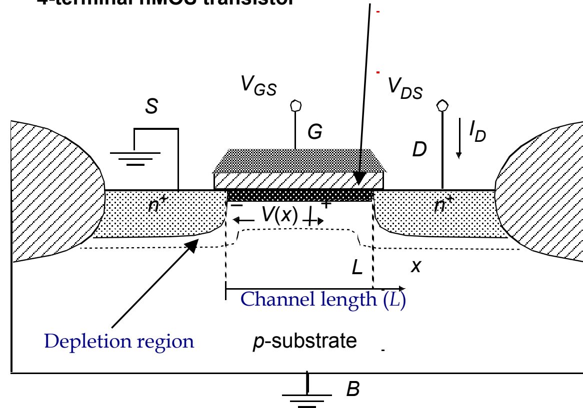
MOS transistor and its bias conditions

- The nMOS in Cutoff Mode
  - $V_{GS} = 0$, i.e., there is no bias voltage applied to the gate.
  - Assume $V_{DS} \geq 0$ – there may a potential between drain and source terminals.
  - No voltage at the gate means to current flows from source to drain.
  - They are effectively insulated from each other by the two pn-junction (diodes) located under the n-wells (for nMOS).
- Behavior
  - The device if "off", or in "cutoff"mode, meaning no current is being conducted across the channel.
  - The transistor acts like an open circuit.

nMOS Transistor in Linear Mode



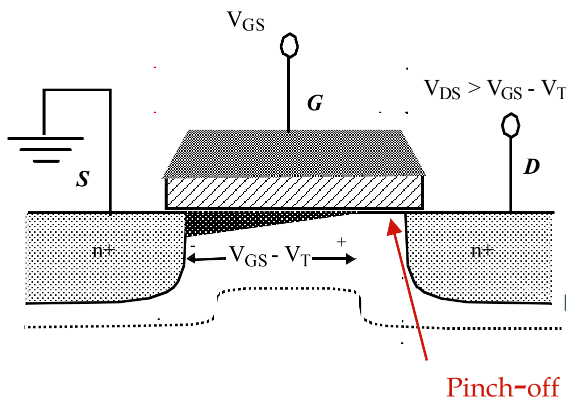
4-terminal nMOS transistor



MOS transistor and its bias conditions

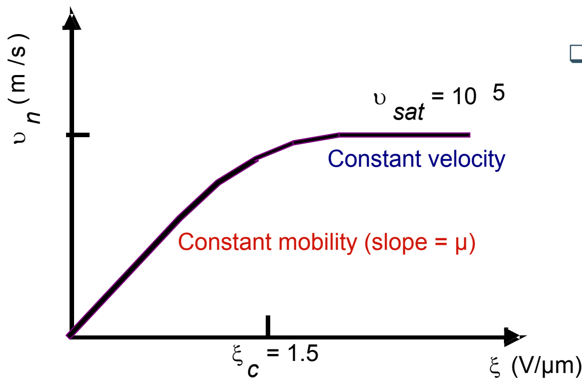
- The nMOS in Resistive Mode
  - $V_{GS} > V_T$ – voltage across the gate is greater than treshold voltage.
  - Assume $V_{DS} > 0$ – there is a potential between drain and source terminals.
  - Voltage difference causes current to flow across the channel, from drain to source.
  - The positive voltage at gate produces an electric field E across the substrate; region "inverts", changing from p-type to n-type (accumulating electrons), providing a conduction path. *Ref: [Weste et al., 1995]*
  - $V(x)$ under the channel $> V_T$, where $0 \leq x \leq L$ (channel length).
- Behavior
  - Over the entire *channel length,* we have a uniform voltage.
  - The transistor acts like a voltage controlled resistor.

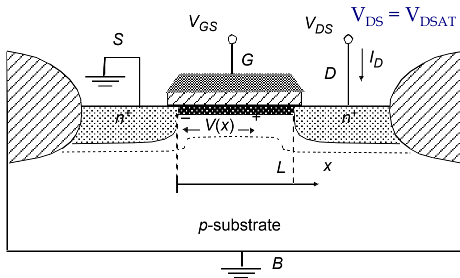
nMOS Transistor in Saturation Mode



- The nMOS in Saturation Mode
  - Channel voltage is not uniform, and becomes less than V_T, i.e. V_{GS} - VT.
  - $V_{GS} – V(X) < V_T$.
  - $V_{GS} – V_{DS} \leq V_T$ or $V_{GS} – V_T \leq V_{DS}$
  - Current remains constant (i.e., "saturates"), and becomes independent of any further applied voltage at the supply V_{DS}.
  - The dependency of the current I_D on V_{GS} is a squared function.
- Behavior
  - Over the entire *channel length,* we have a decreasing thickness, where the conducting channel is pinched off closer to the drain terminal.
  - Charge is injected into the region, flowing to the drain (current flow is in opposite direction of electron mobility).
  - The transistor acts like a voltage controlled current source.

nMOS Transistor in Velocity Saturation

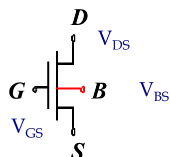




MOS transistor and its bias conditions

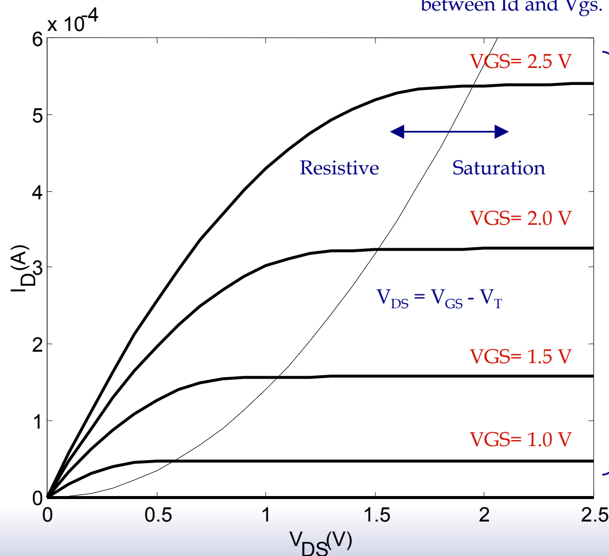
- The nMOS devices with a Short Channel
  - Effective length of channel is modulated by V_{DS}.
  - Increasing V_{DS} causes depletion region at drain terminal to grow, reducing the channel length.
  - The electrical field reaches a transition point, where we enter "velocity saturation", V_{DS} becomes V_{DSAT}.
  - This reduces the amount of current a transistor can deliver for a given control voltage V_{GS}.
  - Reducing the supply voltage V_{DS} doesn't have as much effect for short-channel devices as it does for long-channel ones.
  - Most deep submicron devices can be considered "short channel".

I vs. V – Long Channel nMOS Transistor



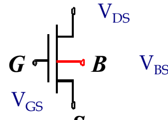
4-terminal nMOS transistor

Quadratic relationship between Id and Vgs.

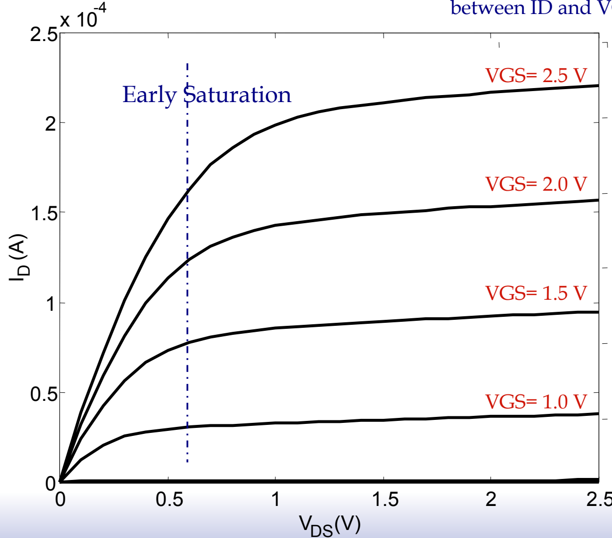


- The nMOS transistor
  - We are interested in the transistor voltages V_{DS}, the *supply voltage*, V_{GS}, the *control voltage*, and V_{BS}, the voltage between the substrate "bulk" and the source terminals.
  - We are also interested in how much current, I_D, we can get to flow from drain to source terminals, due to the difference in potential, V_{DS}, between V_{DD} and V_{SS} (GND), when a biasing voltage, V_{GS}, is applied at the gate terminal.
- Factors
  - The *channel length* and width properties play an important role in transistor performance.
  - Prominent criteria: current sourcing, electric field, required voltages and feature sizing as we scale.

I vs. V – Short Channel nMOS Transistor



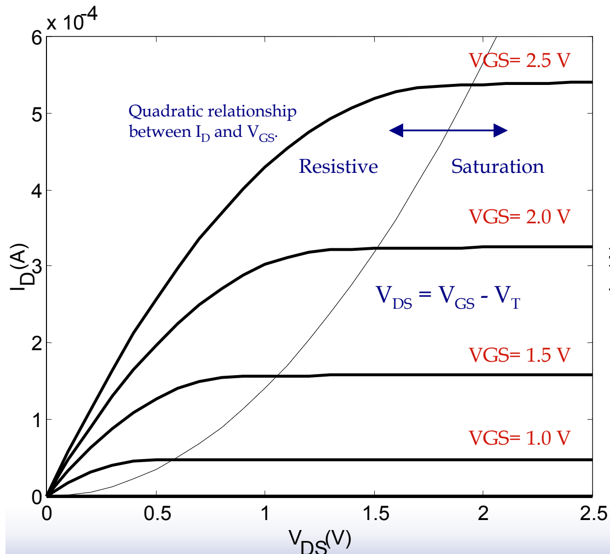
4-terminal nMOS transistor

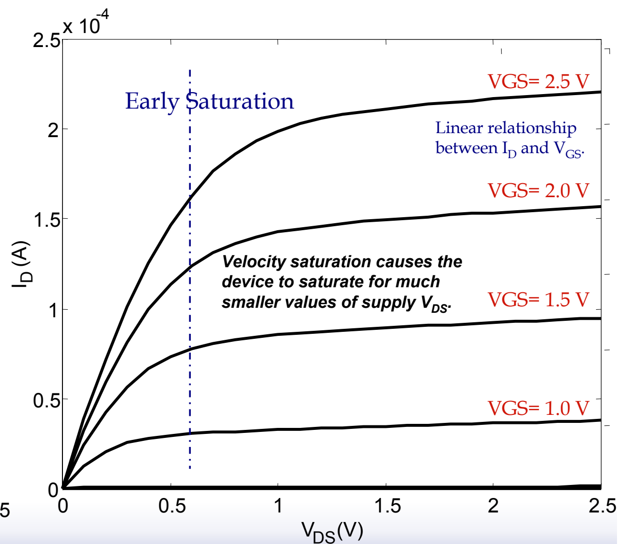


- The nMOS transistor
  - The channel length can effectively be shortened by increasing V_{DS} to the point that depletion region shortens available channel region beneath the gate.
  - Also, deep-submicron fabrication of circuits has shortened the channel length to where this behavior is manifest.
- Factors
  - The *channel length* and width properties play an important role in transistor performance.
  - With a shorter channel length, we aren't able to source as much current through the transistor as we can with a long-channel MOS device (although for pMOS, this is not as much of an issue, because it uses holes rather than electrons as charge carriers).

Long vs. Short Channel nMOS Devices

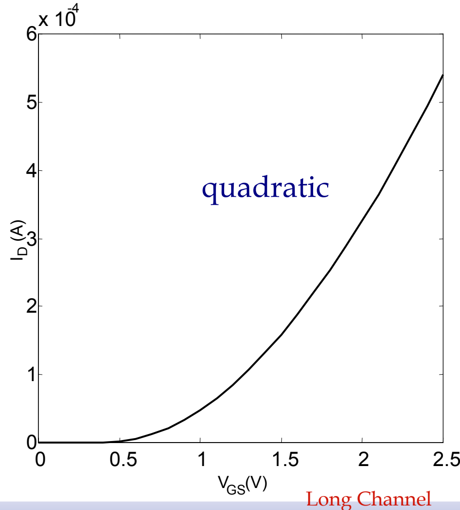
Comparing the two curves, we see: (1) Given a bias voltage across the gate, long channel devices have greater current sourcing capability than short channel devices (~.55 mA vs ~1.6 mA at V_{GS} = ~2.5v) in resistive mode; (2) given a supply voltage, we source more current with the long channel device than the short one (~.55 mA vs ~.225 mA at V_{DS} = 2.5v) in saturation. This affects drive strength, line length, and fan out in the actual design.



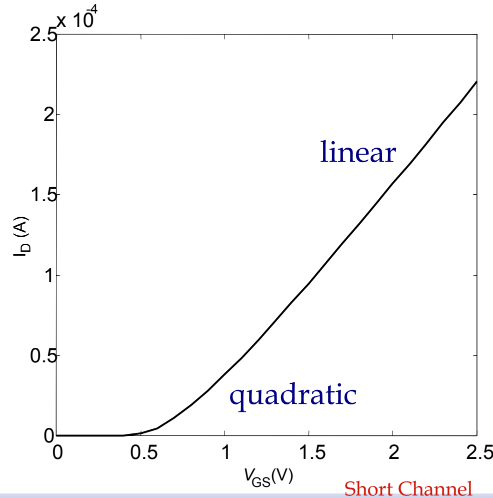


Long vs. Short Channel nMOS Devices

JD: Comparing the two curves, we see: (1) Given a bias voltage across the gate, long channel devices have greater current sourcing capability than short channel devices (as in the previous comparison figure); (2) given a selection of possible CMOS technology libraries, we use such performance curves to evaluate the library models' suitability for use in our design application. Suitability is partially determined, again, by desired drive strength, fan out, line length, etc. The VLSI component engineer must carefully craft higher-level model artifacts from these basic ones, insuring that overall usability of the library elements is well understood and predictable by the EDA tool designers and the VLSI systems engineers.

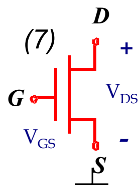


Long Channel



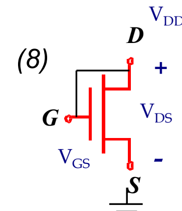
Short Channel

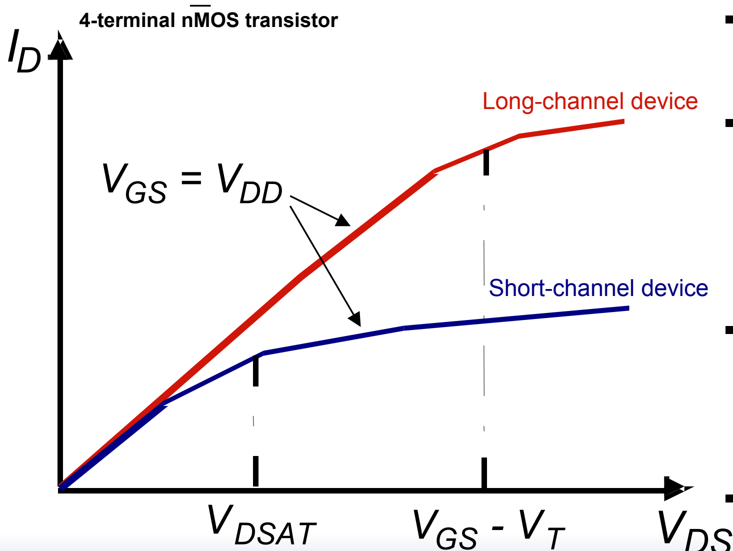
The nMOS Perspective



4-terminal nMOS transistor

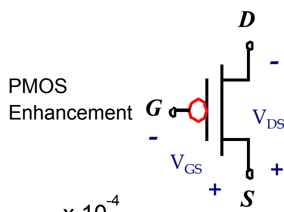
JD: Looking at the case when $V_{GS} = V_{DD}$ (which is the supply voltage.) for different values of V_{DS}.

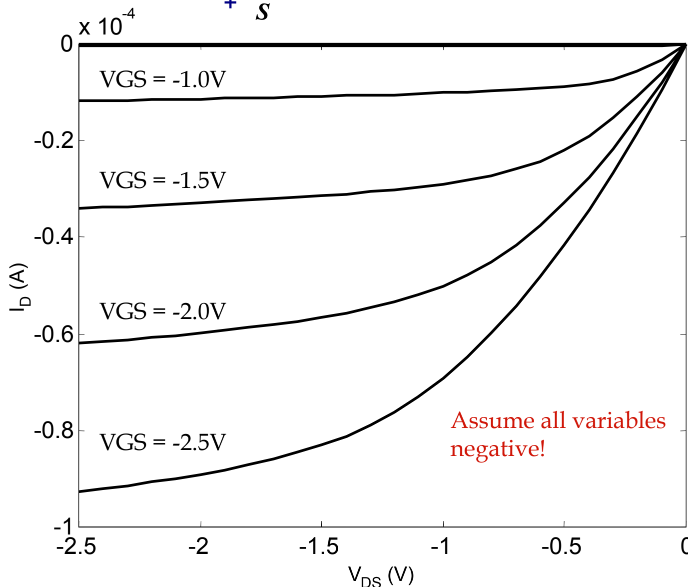




- Objective
  - Give the designer an intuitive sense of the operating behavior of the nMOS (and pMOS) devices.
  - For component library designers, or high-performance CPU designers, this gives a sense of how the dominant design parameters affect performance.
  - In a digital circuit, we're interested in operating region where V_{GS} and V_{DS} are high values, for sourcing maximum available current, given some V_{GS} and V_{DS}.
  - This is when $V_{GS} = V_{DS} = V_{DD}$ (the supply voltage); note this means we are likely tying the gate and drain together (shown above).

The pMOS Transistor



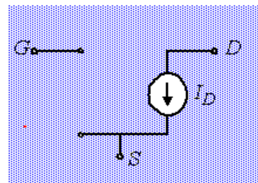


- The pMOS transistor
  - The reversal of n-type and p-type regions yields a p-channel MOS transistor.
  - Applying a negative gate voltage with respect to the source (V_{SS}) draws holes into the region below the gate, resulting in the channel changing from n-type to p-type.
  - A conduction path in pMOS is created between source and the drain.
  - Conduction in the p-channel results from movement of holes, not electrons.
  - A negative drain voltage "sweeps" holes from source through the channel to the drain.
  - Short channel regions as a result of increased V_{DS} do not affect pMOS devices as much.

Ref [Weste et al., 1995]

I-V Relations - Manual Analysis Model

JD: These appear to basically be the same information, culled from two slides and placed on a single one. Not all of the variables and parameters are identified (so you have to read the text for definitions).



Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$V_{DS} > V_{GS} - V_T$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$V_{DS} < V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

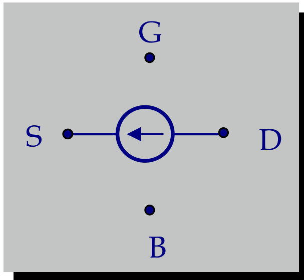
with

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

A "Unified Model" for Manual Analysis

JD: This model is simpler than the one initially developed first by the authors. What is trades in accuracy, it provides in ease of use for manual analysis (and for designer intuition when selecting a library or scaling to a new technology). We'll use this one for any analysis we may be required to do (which some of the HW problems will reference).

JD: V_{GT} is the gate threshold voltage, what we have been calling V_{GS} - V_T. The authors slip this one in very discreetly without telling us.



$$I_D = 0 \text{ for } V_{GT} \leq 0$$

$$I_D = k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \geq 0$$

$$\text{with } V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}),$$

$$V_{GT} = V_{GS} - V_T,$$

$$\text{and } V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

JD: This model does the following: (1) it divides the overall operation space of transistor into 3 regions – linear, saturation, velocity saturation; (2) it defines functional relationships using the voltages at the 4 terminals; and, (3) it uses a set of 5 parameters, whose values we'll predefine for a 0.25 micron CMOS process (see next slide).

Transistor Parameters for Manual Analysis

JD: When we start looking into projects (and possibly some of the homework problems as well for Chapter 3), we'll use these parameters for our analysis as we are carrying out VLSI systems design for high-performance/low power devices at the switch level. Most of the projects will assume a 0.25 micron CMOS process, and you will likely be required to carry out manual calculations (which can be done in MS-Excel for plot comparisons) for some of the design parameters once you have developed your logic switch schematic network and layout topologies for your block designs.

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

Week 3 Summary

- Introduced the MOS transistor
  - Its analog behavior.
  - Its abstraction as a digital switch.
- Modes of operation
  - Relevant in establishing transistor performance characteristics.
  - We need to understand basic device operation, onto which we add knowledge about resistance and capacitance (next week).