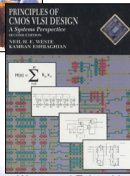


Rabaei, Chandrakasan,
and Nikolic, 2003.



Weste and Eshraghian, 1995.

CMOS Transistor Models

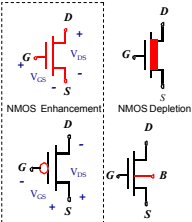
(part 1 – behaviors & parameters)

Adapted/extended by James P. Davis, Ph.D.
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Topics of Week 3

- Discuss the CMOS transistor – this time, we want to look at some of the modeling issues associated with MOS transistors. In a sense, we are elaborating on our basic understanding of the devices—but with a focus on issues that VLSI IC designers must contend with when changing technology due to device scaling.
- This material is from Chapter 3 – Rabaei et al., § 3.3.1, 3.3.2 (first part), pp. 87-106. Slides for Chapter 3, #s 20-36. In areas where the Rabaei text is lacking in clear explanation, I augment with narrative from the Weste et al. text (© 1995 Addison Wesley, Inc.)
- The focus is on 6-7 different aspects of device modeling that are relevant to our set-up of building high-performance, low-power systems out of these devices. The logic argument moves through the assigned reading.
 - However, I found the flow of this material very confusing and somewhat disorganized; it is not clear as to what is the authors' point in this presentation of material.
 - You actually don't get a glimpse of this until the last section of Ch3, so I will present this material in a reorganized fashion, with some references to Weste et al., when points need clarification.

MOS Transistors - Types and Symbols



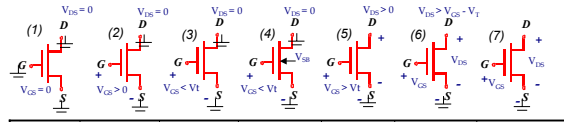
Note: current CMOS device transistors are "enhancement" mode only.

Ref. [Weste et al., 1995]

- The Digital Systems abstraction
 - A MOS transistor is an analog device for which we operate under conditions where we treat it as a digital device (e.g., DC operation).
- The MOS abstraction
 - A "majority carrier" device, the current in conducting channel (between drain and source) is controlled by voltage applied to gate.
 - nMOS – majority carrier is electrons, so a "+" voltage at the gate "enhances" number of electrons in channel, increasing conductivity.
 - pMOS – majority carriers are holes, so "-" voltage at gate "enhances" number of holes in channel, increasing conductivity. Ref. [Weste et al., 1995]
- Enhancement versus Depletion mode
 - Difference between two modes has to do with whether there is a "bias" or voltage difference between the supply voltage, V_{DS} , and the control voltage, V_{GS} .
 - Enhancement mode devices conduct current, I_D , across the channel under the gate when a positive difference (nMOS) or negative difference (pMOS) exists between V_{DS} and V_{GS} . Ref. [Weste et al., 1995]
 - Depletion mode conducts I_D when $V_{DS} = V_{GS}$.

nMOS Transistor – Taxonomy of Scenarios

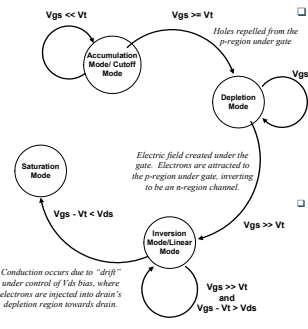
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No gate bias voltage	Small gate bias voltage	Increased gate voltage	Body-bias in substrate	Resistive or linear mode	Saturation mode	Velocity saturation
MOS device is cutoff. High resistance is between drain and source terminals.	Gate and bulk substrate form plates of a capacitor with gate oxide under the gate as the dielectric. It acts like a p-n junction diode; charge is depleted between "plates".	Depletion surface "inverts" to n-type from p-type material. Further increase in V_{GS} has no further effect, but charge concentration in inversion layer increases.	We next look at the body-well bias in the substrate. The bias, V_{BS} , is small, i.e. $V_{BS} > -0.6V$. Bias in the bulk is essential to preserve diodes in well to substrate as "reverse-biased".	Voltage difference cause I_D current to flow, drain to source. The volts under channel is $V(x) > V_t$ for entire length of channel, $0 \leq x \leq L$.	Channel voltage not uniform, less than V_t . $V_{GS} - V(x) < V_t$. Conducting channel pinched off. Channel thickness is gradually reduced (from S to D) until pinch-off.	Increasing V_{DS} (although I_D is independent in saturation), causes E field change. Depletion region grows, shortening channel. Velocity saturation, $V_{GS} \Rightarrow V_{GSAT}$. Reduces amount of I_D transistor can deliver.



Transistor Abstract State Sequence

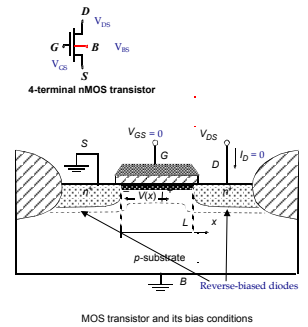


- Transitioning from Cut-off mode to Linear mode
 - We can illustrate this with a state diagram, showing how a gate bias voltage increase causes transitions in the underlying p-region to create a conducting channel between the n-wells in the nMOS transistor.
 - If the inversion under the gate (i.e., in the n-channel) is "weak", then the drain current, I_D , is dependent on the gate and drain voltages (V_{GS} and V_{DS}), and we are operating in "linear" or "resistive" mode.
- Transitioning from Linear to Saturation
 - If the n-channel region is "strongly inverted", as a result of $V_{DS} > V_{GS} - V_t$, and the potential $V_{SD} < V_t$ (the gate-to-drain voltage less than threshold). Channel is "pinched off", not reaching drain. Voltage across channel is $V_{GS} - V_t$, independent of V_{DS} .
 - Note how current I_D is dependent initially on both V_{GS} and V_{DS} , then only on V_{GS} when in saturation mode. Ref. [Weste et al., 1995]

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nMOS Transistor in Cutoff Mode



- The nMOS in Cutoff Mode
 - $V_{GS} = 0$, i.e., there is no bias voltage applied to the gate.
 - Assume $V_{DS} \geq 0$ – there may a potential between drain and source terminals.
 - No voltage at the gate means to "current flows from source to drain."
 - They are effectively insulated from each other by the two p-n junction (diodes) located under the n-wells (for nMOS).
- Behavior
 - The device is "off", or in "cutoff" mode, meaning no current is being conducted across the channel.
 - The transistor acts like an open circuit.



Week 3 Summary

- Introduced the MOS transistor
 - Its analog behavior.
 - Its abstraction as a digital switch.
- Modes of operation
 - Relevant in establishing transistor performance characteristics.
 - We need to understand basic device operation, onto which we add knowledge about resistance and capacitance (next week).
