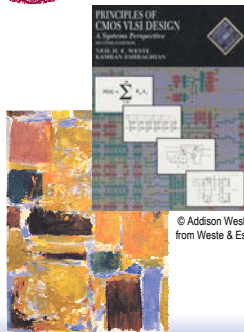




UNIVERSITY OF SOUTH CAROLINA

CSCE 613 – Week-02 Fall 2005

Introduction to CMOS VLSI Design



© Addison Wesley, 1994
from Weste & Eshraghian

From the CMOS Transistor to Gates

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from Rabaey, Chandrakasan & Nikolic

Coverage of Week 2 (CSCE 613)

- Rabaey et al., Chapter 2: § 2.1, 2.2, pp. 36-46.
 - Slides 2- 14
- Rabaey et al., Chapter 3: § 3.3 (3.3.1, 3.3.2), pp. 74-80, 87-90.
 - Slides 3-7, 9, 10 (diodes)
 - Slides 14-22 (MOS transistors)
- Note for coverage of course material
 - As this is CSCE course (and not an EE course), we'll focus more on aspects of device structure, function and behavior that allow us to develop computational models using the constructs at the switch-level of VLSI system abstraction.
 - The EE courses focus more on device characteristics and the circuits aspects of the technology.
 - We may not be covering the Spice-related aspects of modeling devices in this course. We'll focus more on circuit layout and use of design rules.

Topics of Week 2 (from Rabaey)

- Discuss the MOS transistor – behavior, function and structure (materials from Chapters 2 & 3 of Rabaey et al.)
- Discussion of fabrication process (introduction), so we can have some image of the device structure, in situ, along with the device behavior.
- P-MOS and N-MOS transistors -> switching characteristics.
- Introduction of basic device equations
- Introduction of models for manual analysis

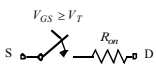
Topics of Week 2 (from Weste)

- Discuss the CMOS transistor – and how we specifically get to gate representations using the basic CMOS composite switch (materials from Chapter 1 of Weste et al., © 1994 Addison Wesley Publishers, Inc.)
- In teaching this course in the past, I have found that students appreciate the material more when it can be related to something they already know—namely, the construction of digital circuits at the gate level, with the tools of Boolean logic.
- We digress from Rabaey et al. to take a look at this material now, as we want to start being able to use it in our journey to higher levels of VLSI system abstraction—using the CMOS switch as the building block for high-performance, low-power circuits for computing systems applications.

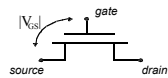
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MOS Transistor - Function

A Switch!



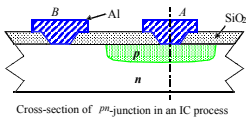
An MOS Transistor



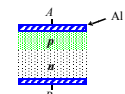
- The MOS (Metal-oxide Semiconductor) transistor
 - Used as the basic "switch" for building gate-level digital logic circuits.
 - As a result of its "bias" properties, it operates either switched ON (logic = 1) or OFF (logic = 0).
- Switching
 - The speed with which a transistor can be switched is a prominent characteristic of the CMOS transistor technology—they are able to switch very fast relative to other MOS circuit technologies.
- Bias voltage
 - We define a voltage value for the threshold so that when the biasing voltage value $V_{GS} > V_T$ then the switch is ON (cf. Lecture 3 slides from Rabaey et al.)
 - A bias voltage causes the flow of current across the transistor; signal paths are created by connecting transistors together.

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The Diode – Introduction



Cross-section of p^n -junction in an IC process



One-dimensional representation

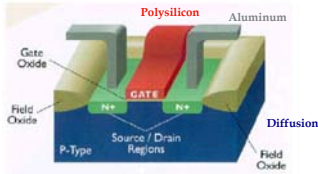


diode symbol

- Diode structure
 - Each MOS transistor contains several reverse-biased diodes that influence its behavior.
 - P-n junction diode: two regions of p- and n-type material, separated by transition region.
 - P-region doped with *acceptor* ions (e.g., boron); holes are the majority carrier.
 - N-region doped with *donor* ions (e.g., arsenic); electrons are the majority carriers.
 - Aluminum provides the contacts for access to p- and n- terminals (A, B).
- Fabrication
 - The p-region forms a "well" within the n-region substrate.
 - Connections to metal contacts are etched through the silicon dioxide insulator material.

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The MOS Transistor - Structure



CMOS device structure

- Layers (1) diffusion (doped silicon), (2) polysilicon (used for interconnect), (3) aluminum, separated by insulating layers.
- N-channel (nMOS) vs p-channel (pMOS) devices are reversed in configuration

4-terminal device

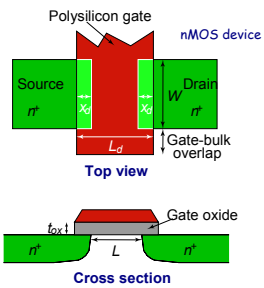
- Voltage applied to the gate terminal determines if and how much current flows between source and drain ports.
- The body is the 4th terminal, serving to modulate device properties.
- When $V_{gs} > V_T$, then a conducting channel is formed between drain and source.
- The larger the V_{gs} , the smaller the resistance of conducting channel, the larger the current.

CMOS device configuration

- P-type transistor: n-type substrate separating 2 "well" areas of p-type material.
- N-type transistor: p-type substrate separating 2 "well" areas of n-type material.
- Current flow for pMOS vs nMOS is under opposite bias conditions.

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MOS Transistor - Structure



P-doped substrate underneath for an n-channel transistor.

Top view

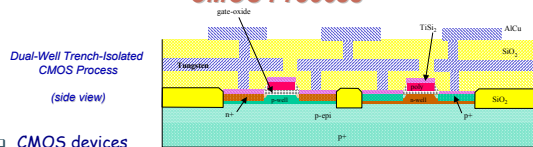
- The polysilicon region rides on top of the diffusion regions, with some overhang.
- The "poly" doesn't sit directly on the diffusion, but is separated by an insulation layer of SiO_2 .
- The length and widths of the regions plays a role in transistor performance.

Cross section view

- The n+ drain and source regions embedded in p-type substrate (nMOS).
- Electron current flows from source to drain through the n-type channel underneath the gate, in the presence of bias voltage (nMOS device as shown).
- Hole current flows from drain to source through the p-type channel for pMOS device.

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CMOS Process



CMOS devices

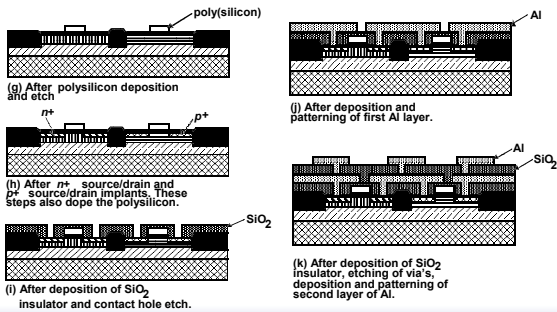
- Use both nMOS and pMOS transistors together to form gate structures.
- Place an n-channel (nMOS) device next to p-channel (pMOS) device, separated by insulator layer to separate the devices.
- Unprogrammed, these devices reside in a "sea of gates" structure, where thousands of devices of each type are arrayed, separated by channels

Process example

- Diffusion layer - uses a p-doped material as a substrate, with epitaxial layer on top of it. Finally, n- and p-doped regions form the substrate regions for individual transistors. The alternately doped p+ and n+ regions form the "well" regions for individual transistors.
- Poly layer - uses a polysilicon created by taking SiO_2 and doping it with more Si to make it conducting rather than insulating.
- Metal layers - multiple layers for different conducting and signal routing paths, used to create elaborate circuit topologies on top of the substrate.

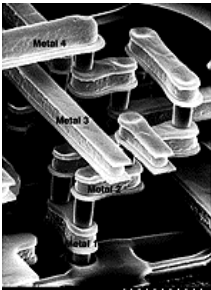
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CMOS Process Walk-Through



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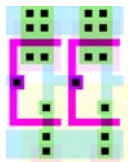
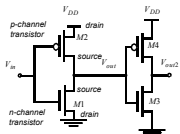
Advanced Metallization



- High-density ICs require many layers of metal to form the interconnect of the circuit.
 - Power V_{DD}
 - Ground V_{SS}
 - Long lines connecting device outputs to next stage inputs.
- As we will see, all of this metal (Aluminum) creates circuit effects that affect load and circuit delay.
 - Resistance
 - Capacitance
 - Inductance
- We can use mathematical analysis to estimate effects.
- We place & route circuits according to design rules.

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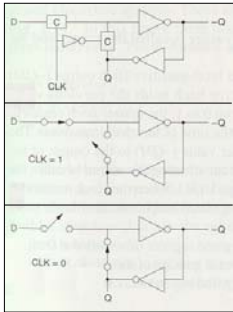
MOS Circuit - Design & Layout



- What is the function of this circuit?
 - This is a signal buffer, created by tying the output of one inverter to the input of another.
 - The inverter is created by tying the source terminals of the p-channel and n-channel transistors together.
 - The gates of both transistors get the bias voltage, but the p- and n- devices are biased opposite of each other.
- Schematic view
 - This shows how the transistors are connected to form the inverter and the buffer driver, placed in the signal path to refresh a signal to its required driving level.
 - Threshold voltage has positive value for nMOS device, negative value for pMOS.
- Layout view
 - This shows the top-level layout of the Buffer driver circuit.
 - The green is the diffusion layers, the red is the poly layer, and the black squares show the contacts for the metal layers.

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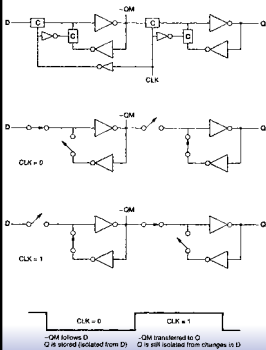
Constructing a CMOS D-Latch



- Structure
 - We can build a "level-triggered" D-latch using a 2-input MUX (built of c-switches) and also using 2 inverters.
 - D is data input, CLK is clock input, and outputs are Q and \bar{Q} .
 - Note that CLK serves as the "S" input to the gates of the p- and n-switch transistors comprising the c-switch.
- Behavior
 - When CLK = 1, Q is set to D, and \bar{Q} is set to \bar{D} (logical NOT).
 - When CLK switches to '0', feedback path around inverter pair is set up, causing current state of Q to be stored.
 - The D input is ignored while CLK = 0.
 - **Level-sensitive:** state of output dependent on level of CLK.

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Constructing a CMOS D-Flip Flop



- Structure (pos edge D-FF)
 - We construct an edge-triggered register by combining two level-sensitive latches in series.
 - The first stage ("master") D-latch is positive sensitive, and the second ("slave") is negative sensitive.
- Behavior
 - While CLK = 0, the master D-latch output, Q_M , follows the D input, while slave D-latch holds its previous value.
 - When CLK transitions 0 \rightarrow 1, master D-latch ceases to sample D input, stores D value at time of transition. The slave latch opens, passing stored value Q_M to output Q_S .
 - While CLK = 1, D in put is prevents from affecting the output, since master is disconnected from D input.
 - When CLK goes 1 \rightarrow 0, the slave latch locks in the master latch output, while master starts sampling D input again.

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Week 2 Summary

- We have looked at the basic MOS device from different points of view:
 - **Structural:** how it is constructed (via fabrication) and what its structure is composed of.
 - **Functional:** how the CMOS devices carry out their switching function, and how we build familiar digital logic functions from combinations of CMOS gates.
 - **Behavioral:** how the CMOS switch is really a 4-terminal device, where there's a reverse bias diode embedded in it that governs its charge carrying behavior.
- Next week: we elaborate the detailed behavior of the MOS gates, and develop appropriate models for analysis, estimation and prediction.

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