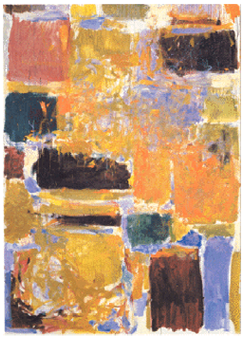

Digital Integrated Circuits

A Design Perspective

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Anantha Chandrakasan
Borivoje Nikolic

Introduction

CSCE 613 – Fall 2005

What is this book all about?

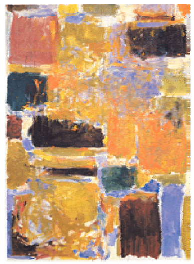
- **Introduction to digital integrated circuits.**
  - CMOS devices and manufacturing technology. CMOS inverters and gates. Propagation delay, noise margins, and power dissipation. Sequential circuits. Arithmetic, interconnect, and memories. Programmable logic arrays. Design methodologies.
- **What will you learn?**
  - Understanding, designing, and optimizing digital circuits with respect to different quality metrics: cost, speed, power dissipation, and reliability

Digital Integrated Circuits

- Introduction: Issues in digital design
- The CMOS inverter
- Combinational logic structures
- Sequential logic gates
- Design methodologies
- Interconnect: R, L and C
- Timing
- Arithmetic building blocks
- Memories and array structures

Introduction

- Why is designing digital ICs different today than it was before?
- Will it change in future?

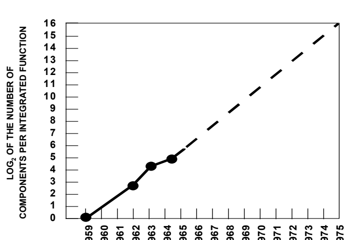


Moore's Law

In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.

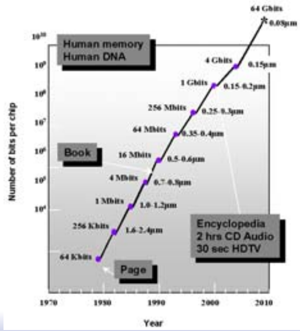
He made a prediction that semiconductor technology will double its effectiveness every 18 months

Moore's Law

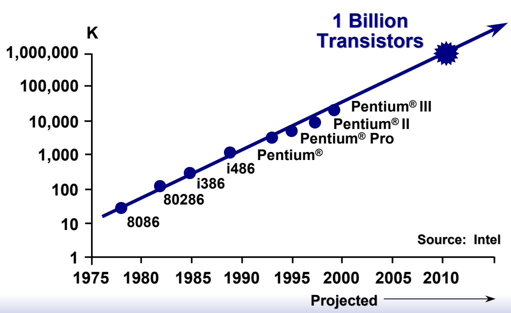


Electronics, April 19, 1965.

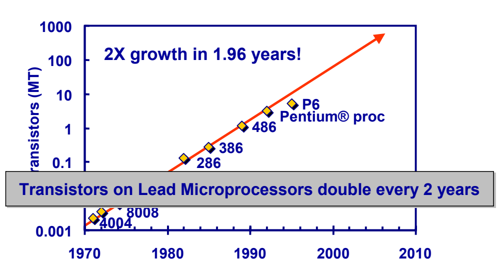
Evolution in Complexity



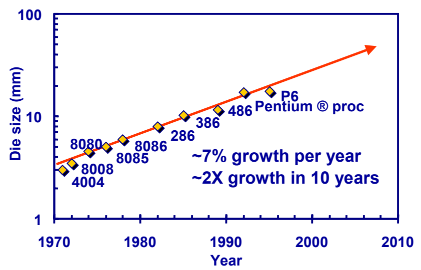
Transistor Counts



Moore's law in Microprocessors

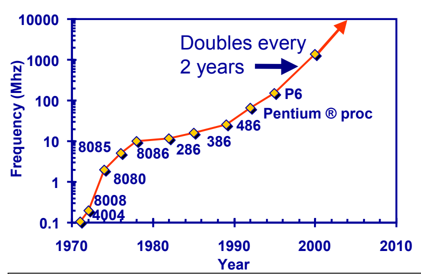


Die Size Growth



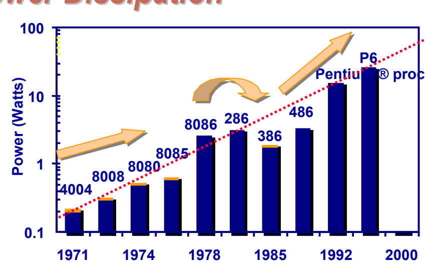
Die size grows by 14% to satisfy Moore's Law

Frequency



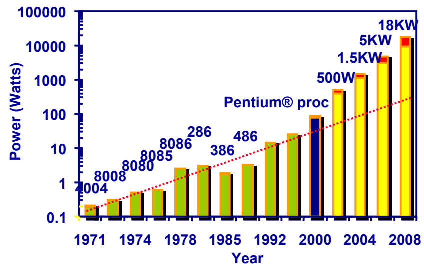
Lead Microprocessors frequency doubles every 2 years

Power Dissipation



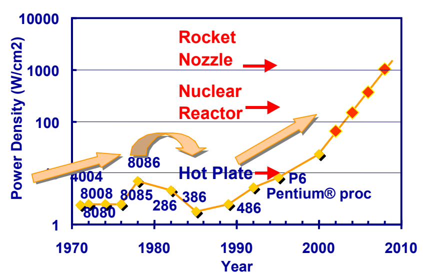
Lead Microprocessors power continues to increase

Power will be a major problem



Power delivery and dissipation will be prohibitive

Power density



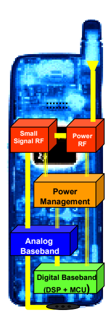
Power density too high to keep junctions at low temp

Not Only Microprocessors

Cell Phone

Digital Cellular Market (Phones Shipped)

	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M



(data from Texas Instruments)

Challenges in Digital Design

∝ DSM

"Microscopic Problems"
- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

Everything Looks a Little Different

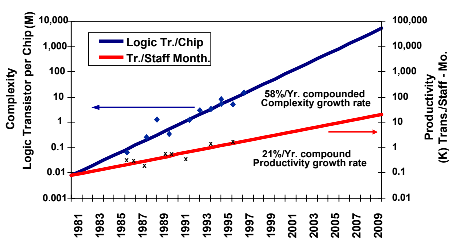
?

∝ 1/DSM

"Macroscopic Issues"
- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

…and There's a Lot of Them!

Productivity Trends

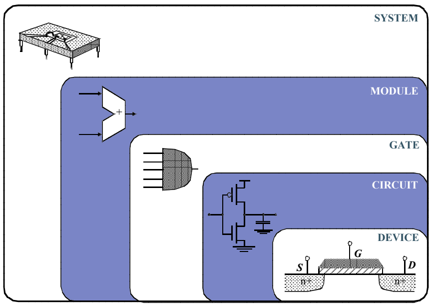


Complexity outpaces design productivity

Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Design Abstraction Levels



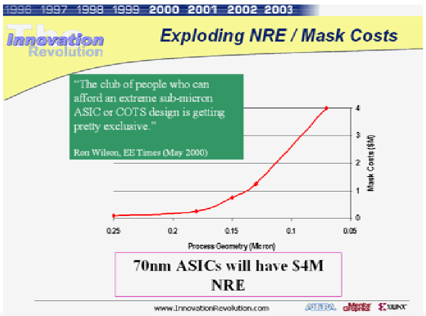
Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

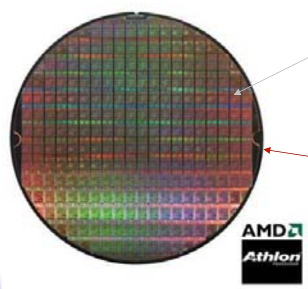
Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
  - design time and effort, mask generation
  - one-time cost factor
- Recurrent costs
  - silicon processing, packaging, test
  - proportional to volume
  - proportional to chip area

NRE Cost is Increasing



Die Cost



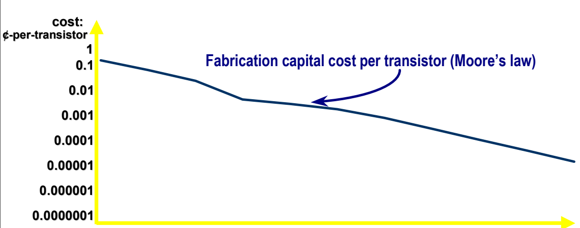
Single die

Wafer

Going up to 12" (30cm)

From http://www.amd.com

Cost per Transistor

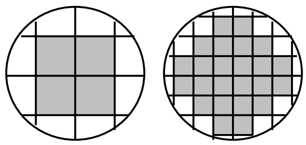


Yield

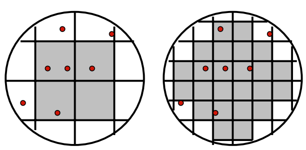
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$



Defects



$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

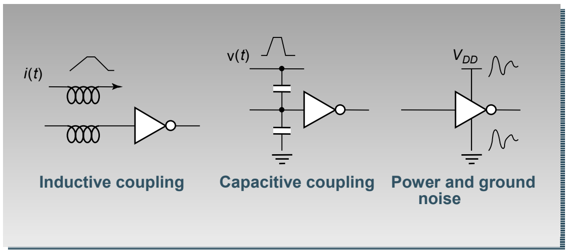
α is approximately 3

$$\text{die cost} = f(\text{die area})^4$$

Some Examples (1994)

Chip	Metal layers	Line width	Wafer cost	Def./ cm²	Area mm²	Dies/ wafer	Yield	Die cost
386DX	2	0.90	$900	1.0	43	360	71%	$4
486 DX2	3	0.80	$1200	1.0	81	181	54%	$12
Power PC 601	4	0.80	$1700	1.3	121	115	28%	$53
HP PA 7100	3	0.80	$1300	1.0	196	66	27%	$73
DEC Alpha	3	0.70	$1500	1.2	234	53	19%	$149
Super Sparc	3	0.70	$1700	1.6	256	48	13%	$272
Pentium	3	0.80	$1500	1.5	296	40	9%	$417

Reliability—
Noise in Digital Integrated Circuits



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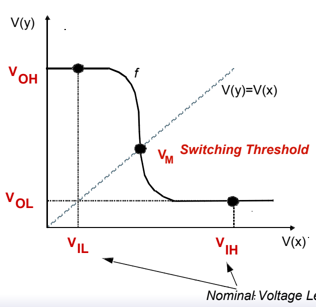
DC Operation
Voltage Transfer Characteristic



VOH = *f*(VIL)
VOL = *f*(VIH)
VM = *f*(VM)

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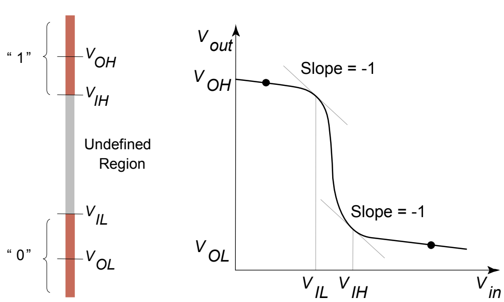
Mapping between analog and digital signals



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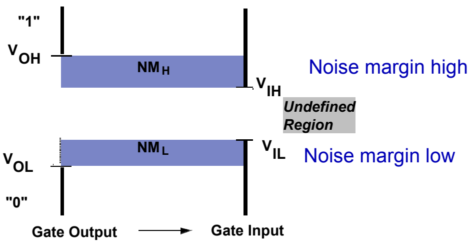
Definition of Noise Margins



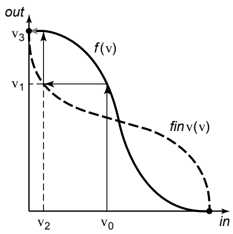
Noise Budget

- Allocates gross noise margin to expected sources of noise
- Sources: supply noise, cross talk, interference, offset
- Differentiate between fixed and proportional noise sources

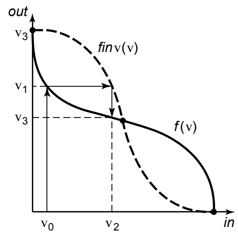
Key Reliability Properties

- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- Noise immunity is the more important metric – the capability to suppress noise sources
- Key metrics: Noise transfer functions, Output impedance of the driver and input impedance of the receiver;

Regenerative Property

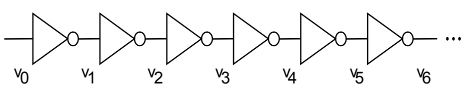


Regenerative

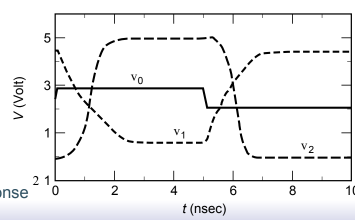


Non-Regenerative

Regenerative Property

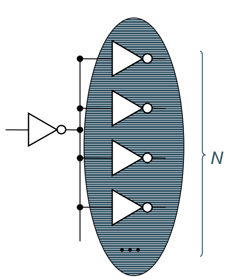


A chain of inverters

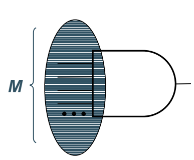


Simulated response

Fan-in and Fan-out

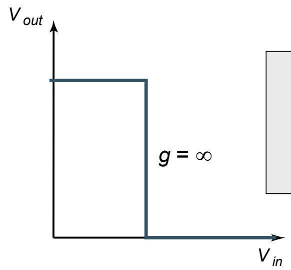


Fan-out *N*



Fan-in *M*

The Ideal Gate



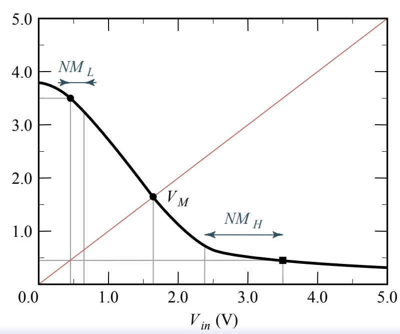
$R_i = \infty$

$R_o = 0$

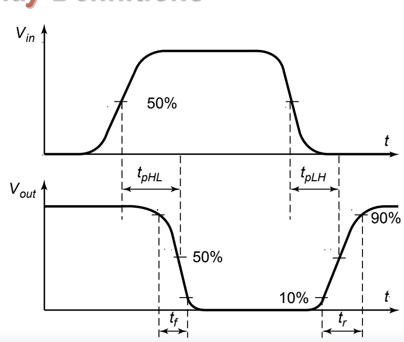
Fanout = ∞

$NM_H = NM_L = V_{DD}/2$

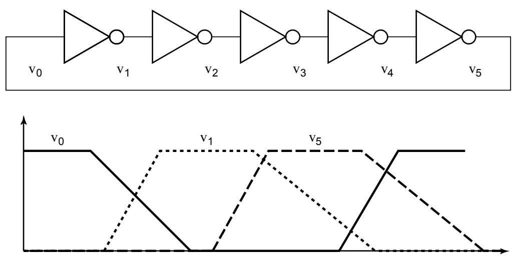
An Old-time Inverter



Delay Definitions

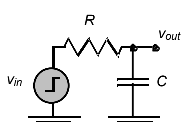


Ring Oscillator



$$T = 2 \times t_p \times N$$

A First-Order RC Network



$$v_{out}(t) = (1 - e^{-t/\tau})\, V$$

$t_p = \ln(2)\, \tau = 0.69\, RC$

Important model – matches delay of inverter

Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply} i(t)$$

Peak power:

$$P_{peak} = V_{supply} i_{peak}$$

Average power:

$$P_{ave} = \frac{1}{T}\int_t^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_t^{t+T} i_{supply}(t)dt$$

Energy and Energy-Delay

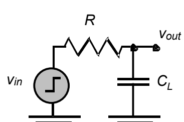
Power-Delay Product (PDP) =

E = Energy per operation = $P_{av} \times t_p$

Energy-Delay Product (EDP) =

quality metric of gate = $E \times t_p$

A First-Order RC Network



$$E_{0 \rightarrow 1} = \int_0^T P(t)dt = V_{dd}\int_0^T i_{supply}(t)dt = V_{dd}\int_0^{Vdd} C_L dV_{out} = C_L \bullet V_{dd}^2$$

$$E_{cap} = \int_0^T P_{cap}(t)dt = \int_0^T V_{out} i_{cap}(t)dt = \int_0^{Vdd} C_L V_{out} dV_{out} = \frac{1}{2} C_L \bullet V_{dd}^2$$

Summary

- Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- Some interesting challenges ahead
  - Getting a clear perspective on the challenges and potential solutions is the purpose of this book
- Understanding the design metrics that govern digital design is crucial
  - Cost, reliability, speed, power and energy dissipation