

CSCE 613

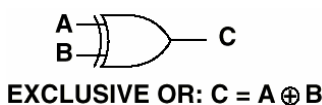
Introduction to CMOS VLSI Design

Fall 2005 – Assignment #7

Layout Design – Performance Characterization

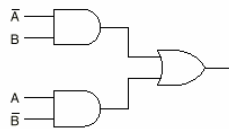
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 Figures: Tanenbaum, 4th ed., © 1999, Prentice Hall Publishers,
 Weste et al., © 1993, Addison Wesley Publishers.
 Rabaey et al. © 2003, Prentice Hall Publishers

CSCE 612 HW #7 – Problem Statement

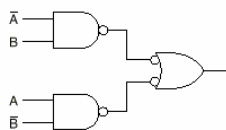


A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

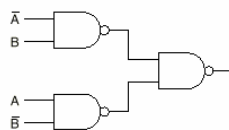
(a)



(b)



(c)



(d)

Source: Tanenbaum, 4th ed. © 1999 Prentice Hall Publishing

□ Circuit Design Topology

- We have a two-stage AND-OR logic network that is connected together, as shown, for XOR.

□ Design Problem

- We want to carry out the following design & analysis tasks in a CMOS process:
 - (a) given some specific values, solve for important parameters affecting performance—(1) parasitic capacitance for the devices and for the lines in the circuit, (2) delay, given the parameters provided by Rabaey et al.
- Carry out some performance analysis on the design by the following:
 - (b) plot appropriate points on performance curves and select best tradeoff point for design elements under consideration.

CSCE 612 HW#7 - Wiring Capacitance Data

We'll use Rabaey et al. Capacitance data for our problem

(data is for a 0.25μ , rather than a 0.5μ , CMOS process, at $V_{DD} = 2.5v$).

Table rows are capacitor's "top plate".
Table columns are its "bottom plate".

Use the Field values for C terms when placing wires over thick field oxide (SiO_2) that isolates different transistors.

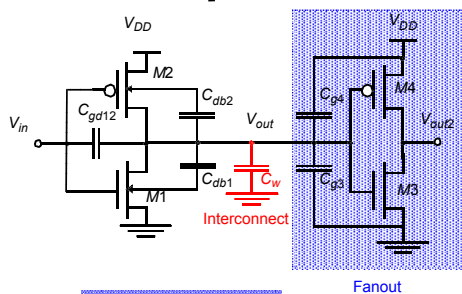
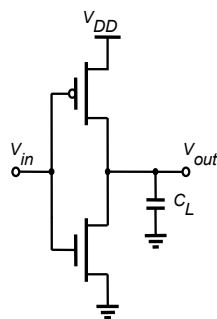
C_{pp} values in upper row.
 C_{fringe} values in lower, shaded row.

Process supports 1 layer Poly and 5 layers Metal.

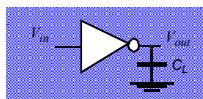
First 4 metal layers Use same H and t_{dr} .
But 5th layer has $H_{m5} = 2H_m$ and $\epsilon_{di5} > \epsilon_{di}$.

	Field	Active	Poly	A11	A12	A13	A14
Poly	88						
	54						
A11	30	41	57				
	40	47	54				
A12	13	15	17	36			
	25	27	29	45			
A13	8.9	9.4	10	15	41		
	18	19	20	27	49		
A14	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
A15	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

CSCE 612 HW#7 - The Inverter Device & Circuit



Simplified Model



Static & Dynamic model

- High and low output levels are V_{DD} and GND.
- "Ratio-less" nMOS and pMOS transistors (logic levels not dependent on transistor sizes)
- Finite R_S resistance between the driving logic source (V_{DD} or GND) and output.
- Low Z_S output impedance, so less sensitive to noise or disturbances.
- High R_L input resistance to the inverter (we'd see this in the 2nd inverter in the Buffer chain of our example).
- No direct path between V_{DD} or GND.

Capacitance

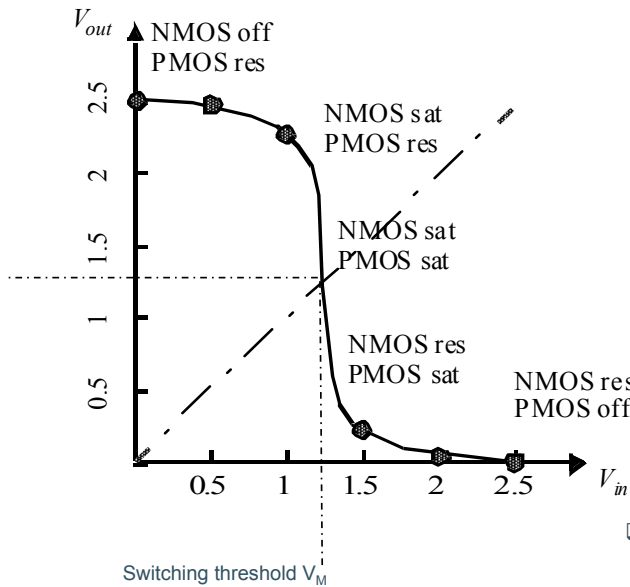
- Assume all device capacitances are lumped into a single capacitor, C_L .
- We have composite C_L : (1) gate-drain, (2) diffusion, (3) wiring, and (4) fan-out load gate capacitances.

- We'll use the Inverter design as the basic cell for our layout problem involving line drivers for the load of a circuit block.

CSCE 612 HW#7 - The Inverter Performance Curve

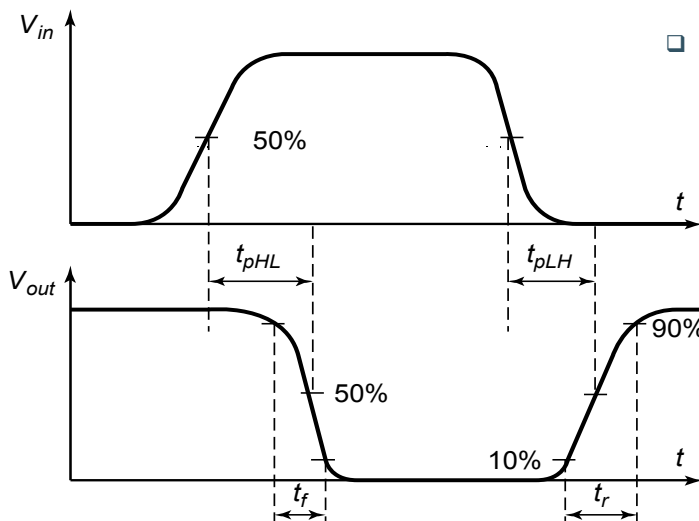
Dynamic (switching) properties

- Using the Voltage Transfer Characteristic (VTC) curve: superimpose those of nMOS and pMOS devices.
- $V_{DD} = 2.5\text{v}$
- The VTC shows a narrow transition zone (i.e., fast switching), due to high gain during switching transient.
- Both transistors are on and in saturation mode. Small change in V_{in} results in large V_{out} variation.
- Switching threshold, V_M is at the point where $V_{out} = V_{in}$.



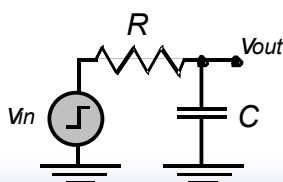
- We'll use this curve to characterize the transistor sizing, then we'll calculate the parameters of the individual transistors.

CSCE 612 HW#7 - The Inverter Performance Curve



Inverter Delay

- Measure propagation of signal from L-H and H-L, between V_{in} and V_{out} , using 50% ($V_{DD}/2$).
- Measure rise and fall times on V_{out} , ranging between 10%-90% V_{DD} .
- Approximate inverter delay by using the first-order RC network (lumped parameter model, Ch 5), solving for time constant, then getting prop. delay.
- We'll solve for t_{pLH} (pMOS) and t_{pHL} (nMOS), finding the transition prop. delays in terms of CL and R_{eqp} and R_{eqn} . These will follow the W_p/W_n ratio of transistors, based on V_M .
- Total t_p is average of $t_{pHL} + t_{pLH}$.

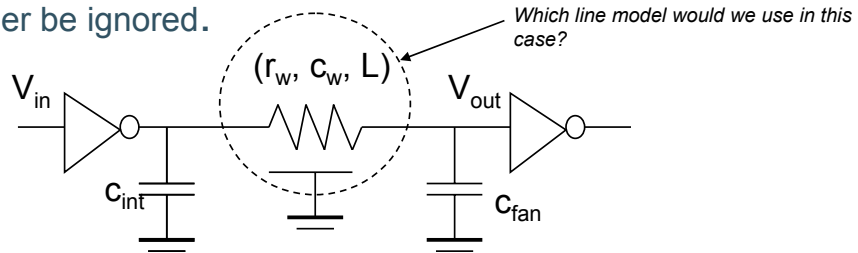


$$v_{out}(t) = (1 - e^{-t/\tau}) V$$

$$t_p = \ln(2) \tau = 0.69 RC$$

CSCE 612 HW#7 - The Wire Between Inverters

- When gates are farther apart, and when they are much smaller than the distances that separate them, wire capacitance and resistance can no longer be ignored.



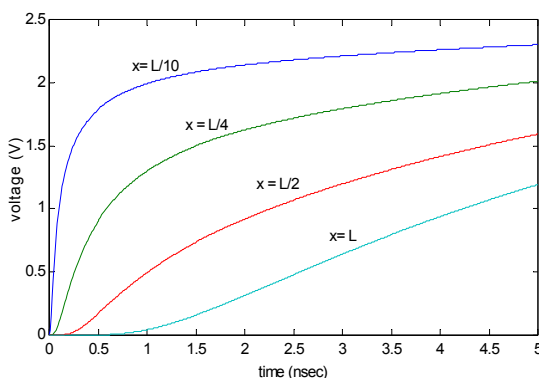
$$t_p = 0.69R_{dr}C_{int} + (0.69R_{dr} + 0.38R_w)C_w + 0.69(R_{dr} + R_w)C_{fan}$$

$$\text{where } R_{dr} = (R_{eqn} + R_{eqp})/2$$

$$t_p = 0.69R_{dr}(C_{int} + C_{fan}) + 0.69(R_{dr}c_w + r_wC_{fan})L + 0.38r_wc_wL^2$$

Source: Irwin&Vijay, PSU, 2002

CSCE 612 HW#7 - The Wire Between Stages



Basic point from the graph: shorter lines have better response than longer ones. Longer lines take longer to reach their driven value, which means the delay of the line affects how long it takes for the signal strength to reach the driven level (here transitioning logic 0 to 1).

Behavior assumption

- We reduce the per-unit-length, ΔL , asymptotically to zero
- Lump total capacitance into single node capacitor to GND.
- Single differential equ., single RC time constant for solution.

Plot meaning

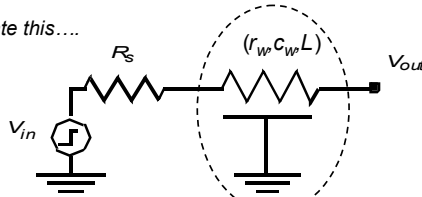
- Response of the rc-wire to an input step function (0 \rightarrow 1).
- V is voltage at a particular point along the wire, and x is distance from the signal source to this point on the wire.
- We see the signal rise times of the unit step response in the distributed rc network, given different line lengths, L.

You have some *minimum* line widths in the design rules, but what *maximum* width should you use?

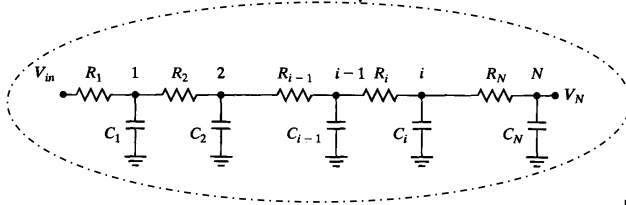
- You'll need to iterate in your analysis on the tradeoff between line widths for L, the resistances, and the capacitances, given the wire between the AND-OR stages.

CSCE 612 HW#7 - The Wire Between Stages

Formulate this....



Like this....



To get this....

$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

$$t_p = 0.69 R_s C_w + 0.38 R_w C_w$$

Behavior assumption

- We have rc -line of length L (not inductance L), driven by voltage source with series resistance R_s representing the driving gate.
- Apply Elmore's formula to obtain approximation of t_p , the total propagation delay from the time constant terms for the network.
- As before $R_w = rL$ and $C_w = cL$ (again, L is wire length).

Delay calculation

- Solve for time constant τ_D in terms of Elmore tree derivation of resistive-capacitive wire (p. 155).
- The delay introduced by wire resistance becomes dominant when: $(R_w C_w)/2 \geq R_s C_w$ or when: $L \geq 2R_s/r$.