

CSCE 613 – CMOS VLSI Design Fall 2005

Description of Project & Deliverables

Introduction

The project assignments come from a selection provided by the text authors, plus some that I have pulled from Parhami (2000) and Flynn and Oberman (2001) texts on Computer Arithmetic. The best way to get into understanding the direct application of the material is to start on the projects. These will be done in teams of two. The projects will have intermediate deliverables--the dates for which will be posted on the web page.

Tutorials on Mentor Tools

Here are some links to tutorials using the Mentor Graphics tools. If you want to use different tools, please feel free to do so, but let me know which tools you will be using. Also, you'll likely need to access Spice, located in all the PC labs on 1st and 3rd floor CSE labs. Completing these tutorials is Assignment #8 (see web page).

http://www.ele.uri.edu/Research/cherry/mentor_tutorial/

<http://www.engr.uky.edu/~ee564/tutorials.htm>

<http://www.ece.unh.edu/courses/ece715/assign/LAB4.html>

Here's a link to a pre-specified design library that is available for use by Mentor university customers, according to the helpful support staff at Mentor. We'll be using this in the projects, so you'll need to take a look.

<http://germanium.ee.wustl.edu/HEP/>

Project Deliverable #1

You need to complete Section 1 of the Project Report (see the Report Template posted on the web page) and turn this in. Follow the guidelines for "efficiency" as noted by the textbook author. Also include any high-level architecture diagrams or gate-level schematics that are appropriate to convey your understanding of the circuit problem and the plan on how your team will solve the problem. *This is an assignment to be completed by the Project teams--one submission per team.*

Get the set of [Project Guidelines](#) (PDF) from the web page, as they have the information about the project teams, assignment, reference materials, timeline, due dates, etc. that you will need to know.

Project Deliverables #2 & 3

You will need to complete the (1) gate level schematic design, and the (2) static, complementary CMOS style switch schematic design. These should both be printed out and turned in. Since the size is likely to cover more than a single sheet of paper, you

should organize your design into the "cell" units that make up the design, clearly labeling the circuit interconnect between logic blocks corresponding to other cell instances of your cell types.

You should also provide me a "taped up" version, that I can walk through with your team, so we can evaluate the quality of the design style according to the design heuristics provided in the Rabaey et al. text, Chapters 5 and 6.

Project Deliverables #4 & 5

You will need to do the following: (1) complete the layout of your CMOS circuit "cells", and (2) carry out some analysis on the performance of the cells--delay, parasitics, and transistor sizing to minimize delay.

Those of you whose projects require an additional optimization for power consumption minimization will also need to make a first pass on this as well.

You will make initial estimates at the cell-level based on the analysis method presented by Rabaey et al., Chapters 5 & 6 in the text.

We'll probably be able to assume that the line lengths within the cell are sufficiently short that will have little effect on the overall calculations--but this should be checked. You can use Spice to check this or do some hand calculations using the assumptions in the text.

Project Deliverables #6&7:

You will need to complete the global placement and routing of interconnect between the cell instances in your design and turn in layout diagrams. In addition, you will need to have completed your analysis of the circuit interconnect for impact on delay and power (for those teams also doing low-power design).

Remember, as a result of interconnect issues, this could require some change to the cells--although a more likely tactic is to change the abutment of the cells, or add inverters to change the drive characteristics of the circuit interconnect.

Final team project report:

Please follow the instructions explicitly, and use the Project Report template for this.

Hopefully, you will have organized your schematic and layout diagrams so that ease of printing is facilitated.

The two analysis components of your report should be presented with the appropriate artifacts, and be clear and concise.

Use the template for your project report: [Project Report Template](#) (Word), as provided on the web page.