

CSCE 613 - Fall 2005
Assignments #6 & 7

Additional Notes

Layout Problem - Part 1

Design a gate schematic for the XOR gate we have been discussing; there are three choices. Select the best architecture and explain why you selected it. See the handouts for Assignment-6 (PDF).

Part 2

Using the Layout rules and text reference materials from Weste et al. (Week #6 Notes), you will perform the hand-layout of the Inverter (NOT), NAND, and NOR Gates, as we have been discussing in class.

Template sheets for the hand-drawn layout can be obtained from the web page. You should be able to layout each gate on one of the sheets, so you'll need three different ones.

Alternately, if you want to use automated tools for the layout, you can create the SOG array structure according to the dimensions of the design rules in Weste et al. and do it using layout tools of your choice (Mentor tools, freeware, etc.).

Part 3

Once you have completed the layout of the individual cells, per above, you will redraw them as "stick" notation (meaning, draw them without regards to the width, etc., as we'll assume for now that the geometries will be the same as what you created for your individual cells using the layout rules).

Use the Circuit Layout Template to lay out the various NAND and NOR gates and Inverters, as required to lay out according to the schematic you created for Part 1.

Please use additional templates for the SOG Cell Layout Template (PDF) and the Circuit Layout Template (PDF), if you need extra copies for doing hand layout of (1) the three devices, NOT, NAND, NOR, and (2) the layout of the gates and wires associated with the XOR gate.

Also: You will need to clearly document the specific layout rules being used for each feature of the circuit geometry (using the examples provided in the Weste et al. text). There is space on the SOG Layout Template for annotating which rules you are using; reference them by number. Please be neat--I will count off points for sloppiness.