

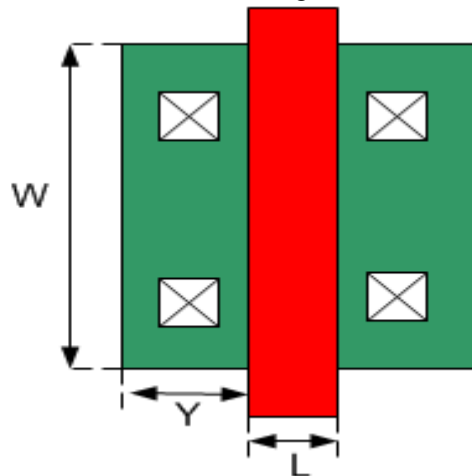
CSCE 613 – CMOS VLSI Design
Homework Assignment #5
CMOS Transistor Modeling and Estimation

These are some additional problems regarding the device modeling, and how we start to consider the parameters for our devices affecting the performance of our circuits. Or, if we look at it the other way around, how our performance targets affect the parameter values we attempt to “push”. Now, we start to consider these parameters in the context of a layout, showing dimensions relative to a specific circuit layout. This is how you’ll start seeing them as we move closer to the course projects.

These problems are from Hodges et al., based on the Chapter 2 materials that we discussed in class lectures from the handouts. Hodges et al. does a better job of presenting this material than the Rabaey et al. text, so we will supplement the material to make sure everyone is getting the gist of how we conduct the analysis, use the operating mode information, and combine terms for using the composite model of capacitance and other parameters.

Problem 1. We have the layout for the transistor as shown in the figure. We have the following values specified for the parameters given the technology we are using: $L = 100 \text{ nm}$, $W = 400 \text{ nm}$, $Y = 300 \text{ nm}$, $K_{eq} = 0.8$, $C_{jb} = 1.6 \text{ fF}/\mu\text{m}^2$, $C_{ox} = 1.6 \times 10^{-6} \text{ F}/\text{cm}^2$, $x_j = 65 \text{ nm}$.

Note, pay special attention to difference in scale of the units of these parameters. Also note: the crosshatched boxes are contacts for drain and source terminals in the diffusion region.



Calculate the Gate and Junction capacitances for this transistor as defined.



Problem 2. We have the following set of parameters for a device: $V_{T0} = 0.4\text{V}$, $\epsilon_c = 6 \text{ V/um}$, $v_{\text{sat}} = 8 \times 10^6 \text{ cm/sec}$, $C_{\text{ox}} = 1.6 \times 10^{-6} \text{ F/cm}^2$, $\mu_e = 270 \text{ cm}^2/\text{V-sec}$, $\gamma = 0.2/\text{V}^2$, $2|\phi_F| = 0.88\text{V}$.

We have two possible sizing scenarios for our NMOS transistor (as shown in the previous figure):

(a) $L = 100 \text{ nm}$, $W = 200 \text{ nm}$.

(b) $L = 100 \text{ nm}$, $W = 400 \text{ nm}$.

We have the voltages as defined as follows: $V_{\text{GS}} = 1.2\text{V}$, $V_{\text{BS}} = 0$, and $0 < V_{\text{DS}} < 1.2\text{V}$.

For each of these two scenarios, and using the parameter values as given above, compare I_D versus V_{DS} for each of the two scenarios (a) and (b).