

CSCE 613 – CMOS VLSI Design
Homework Assignment #1
CMOS Boolean Function Design

The basic material for these problems comes from the Weste and Eshraghian text, as mentioned in the lecture notes. We are interested in gaining an understanding of how we take the basic patterns for connecting p-transistors and n-transistors together, in series and in parallel, and use these patterns to build up CMOS structures for arbitrary logic functions.

Please work the following problems, by drawing your answers, consisting of gate structures configured into circuits, for the following:

1. Design a CMOS circuit-level logic gates implementing the following Boolean functions. Put each function's diagram on a single page, and try to draw clearly, labeling your switch types, your inputs, V_{DD} and V_{SS} , and outputs clearly. Use Visio or other schematic package to draw this if you have access on the department PCs (you might want to create a figure template, as we will be doing some of these again in later assignments).

a. $Z = \overline{A * B * C * D}$

b. $Z = \overline{A + B + C + D}$

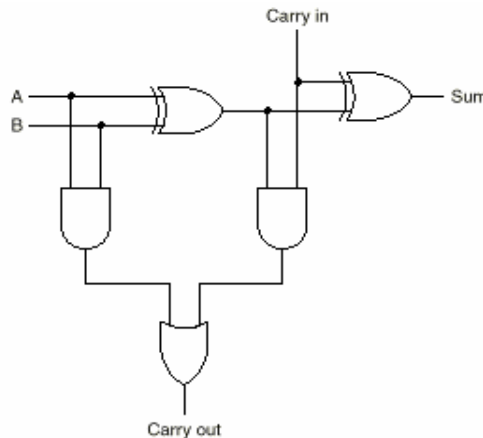
c. $Z = \overline{((A * B * C) + D)}$

d. $Z = \overline{(((A * B) + C) * D)}$

e. $Z = (A * B) + (C * (A + B))$

2. For the given gate-level schematic for the 1-bit Full Adder function, create the CMOS switch-level schematic model. Draw this circuit on a separate page, labeling clearly as for the problems above. *Issue:* how to design the XOR gate?

A	B	Carry in	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Source: Tanenbaum, 4th Edition, ©1999, Prentice-Hall, Inc.