CSCE 491 Lab - Signal/Bus Worksheet

- Use this worksheet to declare your signals and buses for the ASM threads. All threads are inside the scope of Bus Table.

- Note: your Bus Table should have the appropriate buses declared to implement the design function of your circuit.

- Your Bus Table entries will need to have appropriate values for Mode, Type, Element, etc.

- Assume that you have a ^RES signal that is generated externally that is the reset signal for the data registers, and that you have a clock signal CLK for clocking the data registers. You don't need to enter these in the Bus Table.

- We don't need to declare the state registers, since they are implied when we have more than a single state in an ASM thread.

Bus Name	Type	Mode	Element	Width
CLK	Binary	Input	Wire	1
^RES	Binary	Input	Wire	1

Use as many of these sheets as you need to "rough out" your signal declarations.

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Name (Team Name):_____ **Date:**_____

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