UNIVERSITY OF SOUTH CAROLINA

CSCE 491 – Exam #1 Review Sheet
Fall 2003

1. Topics of Coverage

- Algorithmic State Machine (ASM) design of digital hardware systems.
- Design methodology and notation – ASM diagrams, states, conditions, case (multi-way branching), conditional outputs.
- Moore/Mealy style of state machine design
- Registered versus non-registered (i.e., wire) signals and buses.
- Control versus datapath design (single-state models versus multi-state models)
- Clocking and cycle-level delay through digital circuit blocks (both control path and datapath).
- Patterns and mechanisms of concurrency – parallelism, delegation, handshaking, pipelining between state machine threads and their associated data path blocks.
- Macro-function units, register-transfer assignment (either between buses, or through macro-function blocks); nesting of macro-functions.

2. Problem Set

- Analysis and design of ASM model of a digital system – spec to ASM, multi-thread model. Including description of the model's signal inventory (Bus Table).
- Analysis of ASM model output – thread to waveform response, given set of inputs.
- Analysis of a data path circuit – represent as a corresponding set of assignment statements, possibly involving nesting of macro-functions.
- NOTE: this exam focuses on the ASM design method and notation, NOT on the idioms or idiosyncrasies of the flowHDL® tool set. So, thread bounding boxes, label pointers and sub-flow diagrams are not part of the exam's scope.

3. Problem Examples