

CSCE 613 Fundamentals of VLSI Chip Design

Spring 2002

Course Description: In this course, we will study the fundamental structures of VLSI Systems at the lowest levels of system abstraction, namely those associated with the direct application of VLSI devices to particular problems of interest. At its most basic level, VLSI design is concerned with the set of principles governing MOS (metal oxide semiconductor) devices and their behaviors. We start by looking at the CMOS transistors (n-channel and p-channel) and the ways in which we can use them to create the most basic structure—the digital switch. We can proceed to build a range of VLSI structures from this switch, including NAND/NOR gates, Multiplexers, Latches and Registers. Continuing in a bottom-up fashion, we can examine the structure of more complex VLSI design components (those at Digital Logic and Register Transfer levels of abstraction) using these primitives.

While learning how to construct fundamental VLSI systems structures from primitive circuit structures, we also will learn about the processes associated with fabricating CMOS devices. Using CMOS as our technology, we examine the circuit level design rules associated with circuit geometries and their layout according to a set of process technology-specific design rules. We also look at factors affecting design: capacitance, clocking, delay and power.

Finally, we will develop a complete picture of the VLSI systems design flow, starting at the Systems level, proceeding through the Register Transfer Level, to the Digital Logic, Circuit and the Device Geometry levels—therefore having a complete picture of the VLSI systems architecture and engineering design process and associated design methods.

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Office Hours: MW 3:00 – 5:00; TTH 1:30 – 2:00.

Time: MWF 1:25 – 2:15PM (Room 2A19, Swearingen)

Text: Neil H. E. Weste and Kamran Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective (2nd edition)*, Addison Wesley: Reading, MA, 1993.

Grading Policy:	<i>Homework:</i>	30%
	<i>Examinations:</i> Two exams	30%
	<i>Design Project:</i>	40%

Course Structure: *Chapter 6 – CMOS Design Methods: Sections 6.1 – 6.2*
Chapter 1 – Introduction to CMOS Circuits: Sections 1.1 – 1.5
Chapter 6 – Sections 6.3 – 6.6
Chapter 3 – CMOS Processing Technology: Sections 3.1 – 3.4, 3.6
Chapter 4 – Circuit Characterization and Performance Estimation: Sections 4.1 – 4.8
Chapter 5 – CMOS Circuit and Logic Design: Sections 5.1 – 5.3, 5.5 – 5.7

Project: 802.11/802.3 Wireless LAN domain

We will identify, partition and design portions of the 802.11 MAC layer as an application-specific semi-custom VLSI structure (rather than using a CPU IP embedded core). This will start at the system-level, proceeding through RTL and logic levels until reaching the circuit and physical geometry definitions.

Project: Custom Design, Place & Route of Xilinx Vertex FPGA blocks

As an alternate project topic, we'll take the Xilinx Vertex FPGA architecture and create gate-level and circuit-level realizations using *Magic 7.1* place and route tools. Selected Xilinx applications will be used as the basis for project.