A Low-Swing Differential Signaling Scheme for On-chip Global Interconnects

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***Abstract*— The dense Very Deep Submicron (VDSM) System on Chips (SoC) face a serious limitation in performance due to reverse scaling of global interconnects. Interconnection techniques which decrease delay, delay variation and ensure signal integrity, play an important role in the growth of the semiconductor industry into future generations. Current-mode low-swing interconnection techniques provide an attractive alternative to conventional full-swing voltage mode signaling in terms of delay, power and noise immunity. In this paper, we present a new current-mode low-swing interconnection technique which reduces the delay and delay variations in global interconnects. Extensive simulations for performance of our circuit under crosstalk, supply voltage, process and temperature variations were performed. The results indicate significant savings in power, reduction in delay and increase in noise immunity compared to other techniques.**

I. Introduction

An unprecedented level of integration, in terms of both process and functionality, has been achieved in Systems-on-Chip (SoC). However, as a result of the increasing logic and die sizes, the lengths of global interconnects that span the length of the chip do not scale significantly leading to the phenomenon of reverse scaling of interconnects [1]. The higher wire resistance, increased length and decreased wire spacing cause the wire delay to increase considerably compared to gate delay [2]. Hence, delay variations caused by various sources of noise, which includes crosstalk and supply voltage variation, can affect performance of the system significantly and lead to functional errors. The optimal repeater insertion technique [3]–[5], which uses voltage-mode signaling, was developed to reduce the wire delay and improve performance of lengthy global interconnections by breaking them into smaller sections. In this technique, repeaters are inserted at appropriate intervals on the lengthy global interconnect. This makes the quadratic dependence of delay over wire length move towards a linear one. However, with the increase in number and density of the wires with each new technology, the number of repeaters necessary would increase manifold, presenting significant overhead in terms of power and area. Hence, there is a need for a new interconnection scheme that reduces wire delay, its variation and increases noise immunity.

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Low-swing current-mode signaling has unique advantages in terms of power, delay and noise immunity over the conventional voltage mode techniques [6]. Though this technique was widely used for off-chip interconnects [7] and for sensing memory bitlines [8], [9], designers now see its potential for on-chip interconnections too. Current-mode interconnection schemes can be broadly classified as single-ended and differential schemes. Recently, plenty of attention has been given to signaling techniques that operate in current-mode. This includes work done by Burleson [10], Rabaey [11] and Zhang [7]. Differential current-mode schemes have a distinct advantage over the single-ended ones in terms of noise immunity and signal integrity, which is of prime importance in the VDSM designs. This makes the additional overhead in power and area presented by the differential schemes tolerable. Hence, in this paper we consider only the differential current-mode schemes and analyze them. We propose a new current-mode low-swing interconnection scheme that has significant advantages in terms of delay, power and noise immunity compared to other techniques. It has been simulated for variations in supply voltage, process and temperature and the results indicate reliable performance.

This paper is organized as follows. Section II explains the working of current mode signaling schemes and how they influence performance of the system. Section III describes our circuit and explains the functioning of the interconnection scheme. Section IV details the simulation setup and the results obtained. Section V concludes this paper.

II. Current Mode Signaling

The signal transmission system used in CMOS circuits can be broadly classified into two categories: voltage mode signaling and current mode signaling. The important difference between the two transmission systems lie in the signal that in forced on the transmission line, namely the interconnect. While voltage mode uses voltage as the signal, current mode uses the current. A generic circuit for each of these strategies is shown in Fig. 1.

As shown in Fig. 1, voltage mode circuits transmit voltage as the signal on the transmission line, which is received by a voltage mode receiver with infinite input impedance. The voltage has to swing rail-to-rail over the entire length of the transmission line, charging and discharging the line capacitance in a very short amount of time. This leads to large transient currents consuming more power and it also generates power-supply noise [6]. Current mode circuits consist of a

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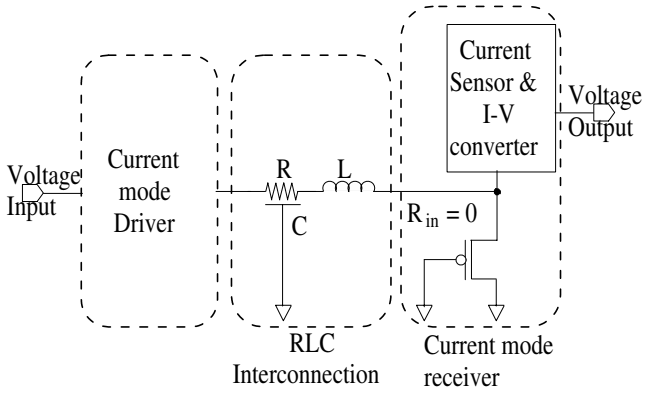
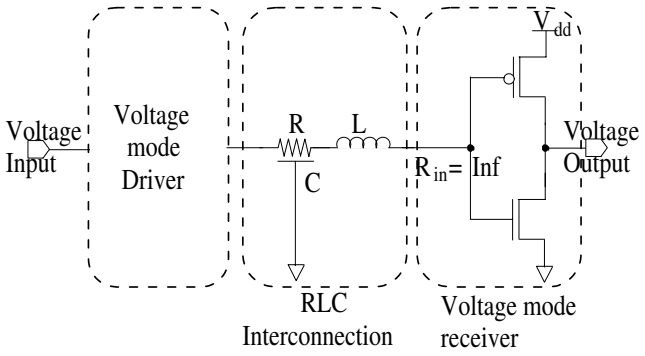


(a) Current mode circuit



(b) Voltage mode circuit

Fig. 1. Generic Current mode and Voltage mode Circuits

current source at the transmitter that sends a current signal on the transmission line, which is received by a matched low impedance current mode receiver. Operating the transmission line in current mode allows voltage swing to be reduced without separate voltage references and isolates the received signal from power supply noise [6]. It also translates into increased bandwidth performance [12] and higher noise immunity.

A good signaling technique is one that provides higher noise immunity and bandwidth, while minimizing power dissipation and delay [6]. For these reasons, current mode signaling technique is a better alternative to voltage mode technique, for the future multi-GHz, noise-prone VDSM chips.

A. Differential and single ended current mode signaling

The CMOS current mode signal transmission system can be further classified into two broad categories: differential current signaling and single-ended current signaling. The important difference between the two techniques is that while differential signaling uses two wires to transmit the same signal, single-ended signaling uses only one. Compared to voltage mode signaling, differential current signaling has reduced delay and higher common-mode noise rejection. Though differential schemes utilize two wires per transmitted signal compared to a single wire in the single-ended schemes, the improvement in performance and power is larger than this overhead. Hence in this work we have developed an on-chip global interconnect signaling scheme, based on the differential current mode signaling techniques. The details of the circuit are presented in the next section.

III. Circuit Details

A. The Driver Circuit

Traditional low-swing drivers use additional reference voltages to produce a low-swing signal output [11]. This overhead is overcome in our driver circuit, the Self Level Converter (SLC) driver, which converts the input full-swing voltage signal into a low-swing signal without requiring additional reference voltages.

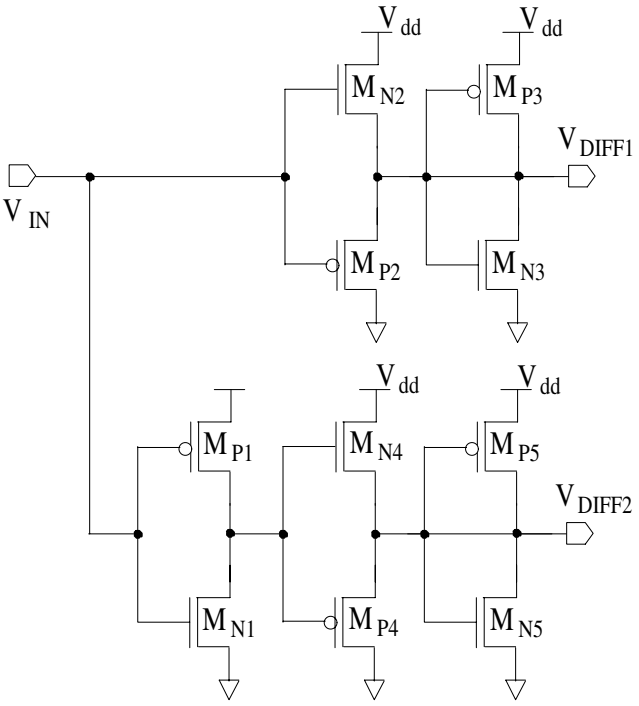


Fig. 2. Self Level Converter Driver Circuit

The SLC driver consists of a pair of identical level converter circuits fed by the input signal and its complement, as shown in Fig. 2. The transistors M_{P2} and M_{N2} are connected in a source-follower configuration. The output voltage of this pair swings between $V_{dd} - V_{thn}$ (high) and $GND + V_{thp}$ (low), and is fed to a diode connected pair of transistors M_{P3} and M_{N3}. These transistors can be sized appropriately to control the output voltage swing in the desired range. To produce the differential complement of this signal, the full-swing input signal is inverted and fed to a similar level shifter configuration formed by transistors M_{P4}, M_{N4}, M_{P5} and M_{N5}. The low-swing differential outputs V_{DIFF1} and V_{DIFF2} are obtained at the output of the level converters and transmitted over the

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interconnect.

The SLC driver is sized such that the voltage obtained on the interconnect varies from 650mV to 850mV, with a swing of about 200mV. The current swing is seen to be around $160\mu A$. To increase noise immunity and decrease the effect of inductance, the wires transmitting the differential signals are laid out as a tightly coupled twisted wire pair similar to the Twisted Differential Line (TDL) scheme [13].

B. The Receiver Circuit

The receiver circuit is based on the Asymmetric Source Driver Level Converter (ASDLC) [11] scheme. Though this circuit exhibits low delay and high noise immunity, being a single-ended signaling scheme, the ASDLC technique has scope for further reduction in delay, increase in noise immunity and common mode rejection [6]. Hence, a new current-mode low-swing differential circuit called the Modified Asymmetric Source Driver Level Converter (MASDLC) circuit, which is based on the ASDLC circuit has been developed. It has increased noise immunity and lower delay variation compared to other circuits. The MASDLC circuit is shown in Fig. 3.

The signals V_{DIFF1} and V_{DIFF2} transmitted over the differential pair of interconnect lines are input to the MASDLC receiver circuit. The receiver amplifies the received signal, generates the difference between them and amplifies it to reproduce the full-swing voltage signal input to the SLC driver. The interconnect line carrying V_{DIFF1} (V_{DIFF2}) is terminated at the drain of transistor M_{N2} (M_{N7}). Transistor M_{N2} (M_{N7}) is biased by the diode connected transistor pair M_{P1} and M_{N1}. At this point, to increase stability of the bias of transistor M_{P3} (M_{P6}), the signal is passed through a common-gate stage formed by transistors M_{N2} (M_{N7}) and M_{P2} (M_{P7}), instead of passing them through a cross-coupled inverter pair as in the ASDLC scheme. The diode-connected transistor M_{P2} (M_{P7}) is sized such that its V_{DS} is enough to provide the gate voltage for transistor M_{P3} (M_{P6}). The signal is again passed through another amplifier, a common-source amplifier, formed by transistors M_{P3} (M_{P6}) and M_{N3} (M_{N5}). The transistors M_{P3} (M_{P6}) and M_{N3} (M_{N5}) are sized to provide a large transconductance which aids in sensing minute changes in the respective gate-source voltages. The amplified signals obtained from the inputs V_{DIFF1} and V_{DIFF2} are fed to each side of the current mirror formed by transistors M_{P4} and M_{P5}. The output of the current mirror is the difference of these signals, obtained at the drain of transistor M_{N5}. Since the receiver produces a difference signal, it cancels out any coupled and common mode noise that may be present in the signal. This output is then passed through an inverter stage (transistors M_{P8} and M_{N8}) to produce a full-swing output.

A notable feature of this circuit is that it makes use of both common-gate and common-source amplifier stages thus significantly improving sensitivity. The gain of this circuit is determined by the transconductance of transistors M_{P3}, M_{N3}, M_{P6} and M_{N5}. The current mirror formed by transistors M_{P4} and M_{P5} helps stabilize the dc output at the drain of transistor M_{N6} which balances the amplifier. The combination of TDL wire layout and MASDLC receiver increases the robustness and reliability of this scheme. The various sources of noise that the interconnect is exposed to affect the tightly coupled twisted pair symmetrically, thus translating into common mode noise. Since the MASDLC receiver generates the difference of the two input signals, common mode noise including crosstalk cancel out. This scheme can effectively guard against coupled noise from full-swing aggressors, as seen from the simulation results.

IV. Simulation Setup and Results

Extensive simulations have been performed to evaluate the Twisted Differential Line - Modified Asymmetric Source Driver Level Converter (TDL-MASDLC) scheme in terms of wire delay, delay variations, noise immunity and reliability. The simulation setup consists of three parts. In the first part, the TDL-MASDLC scheme has been compared with the Modified Clamped Bit Line Sense Amplifier (MCBLSA) and the Optimal Repeater Insertion (ORI) schemes in terms of delay, power and noise immunity for various lengths of interconnects. In the second part, the high noise-immunity and reduced delay variation in the TDL-MASDLC scheme is analyzed by extensive simulation under various conditions of coupled noise. The third part consists of simulations to test the reliability of the TDL-MASDLC scheme against variations in process, temperature and supply voltage.

A. Comparison of TDL-MASDLC with other schemes

The simulation setup consists of TDL-MASDLC, MCBLSA and ORI drivers, driving 1GHz pulses through $2\mu m$ wide metal 5/6 interconnects of lengths ranging from 0.2cm to 1.6cm laid out in $0.18\mu m$ technology and terminated by the respective receiver circuits. The delay and power consumed in each of these cases for the three schemes has been shown in Table I. The delay and average power in each of these schemes has been compared and plotted in Fig. 4 and Fig. 5. As can be seen from these figures, the delay of low-swing schemes is less for shorter wire lengths and becomes larger than that of the full-swing scheme for lengths greater than 1.2cm. However, the total average power consumed in the wire and receiver does not increase significantly with wire length as it does in the ORI scheme. The results also indicate that the TDL-MASDLC scheme performs better in terms of power and delay compared to both, the ORI and MCBLSA schemes.

To test the crosstalk noise immunity of these schemes, three closely spaced $2\mu m$ wide interconnect wires of length 1cm were laid out in $0.18\mu m$ and pulsed at 1GHz. The phase of the outer interconnects was opposite to that of the inner wire. While the outer wires were driven using full-swing voltage drivers, the inner wire was driven by one of the three schemes mentioned above. The delay varied by 68%, 33% and 23% for the ORI, MCBLSA and TDL-MASDLC schemes respectively. As mentioned earlier, this result establishes the significant advantage of the TDL-MASDLC scheme over the MCBLSA and ORI schemes in terms of its high noise immunity. To bring out the noise immunity characteristic of the TDL-MASDLC scheme clearly, various cases have been simulated. A description and the results obtained in each of these cases is given below.

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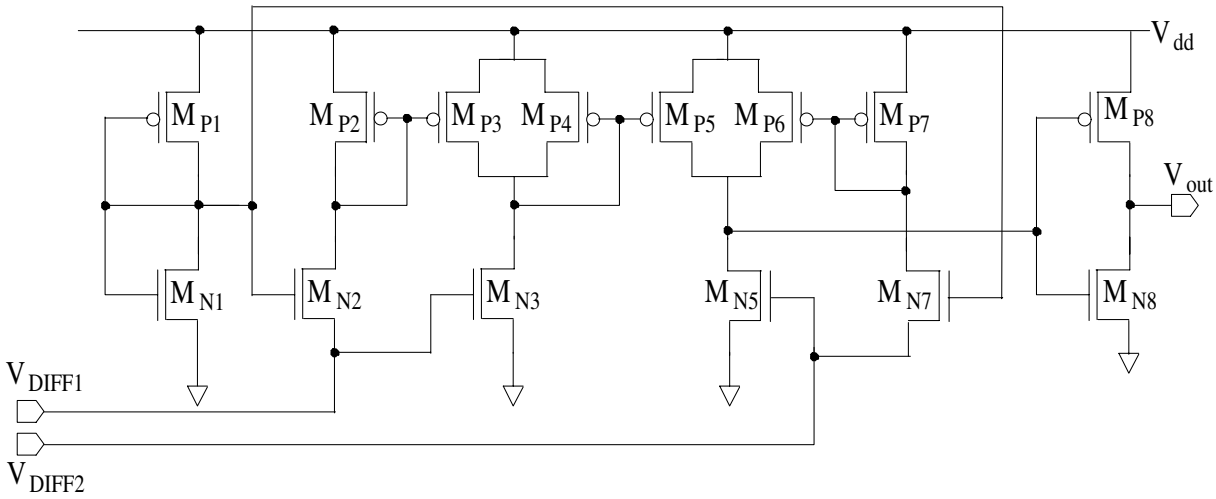

Fig. 3. Circuit Diagram of the MASDLC Receiver Circuit

TABLE I
DELAY AND POWER COMPARISON OF ORI, MCBLSA AND TDL-MASDLC SCHEMES

Wire Length (cm)	ORI Delay (ps)	ORI Avg. Power (mW)	MCBLSA Delay (ps)	MCBLSA Avg. Power (mW)	TDL-MASDLC Delay (ps)	TDL-MASDLC Avg. Power (mW)
0.2	187.483	0.507	117.68	0.2216	106.46	0.215
0.3	205.573	1.645	140.386	1.3957	120.475	1.3161
0.5	325.385	3.047	259.68	2.038	246.55	1.9160
0.7	441.574	5.837	282.85	3.0547	264.478	2.8211
1.0	497.54	7.835	441.404	3.536	429.57	3.4404
1.2	584.683	9.374	573.58	3.956	540.938	3.7326
1.4	671.526	12.3543	689.57	4.294	664.68	4.155
1.6	786.48	13.547	825.483	4.638	805.385	4.5846

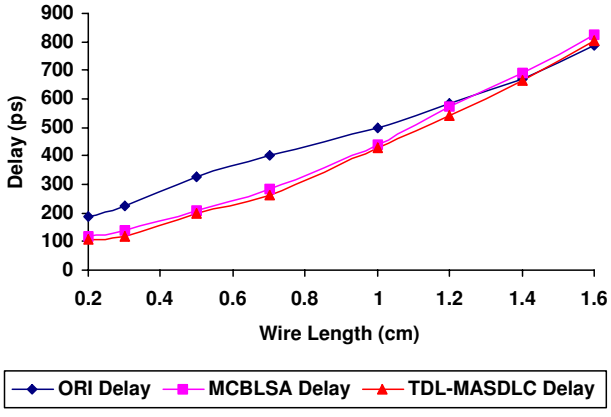

Fig. 4. Delay Comparison of ORI, MCBLSA and TDL-MASDLC Schemes

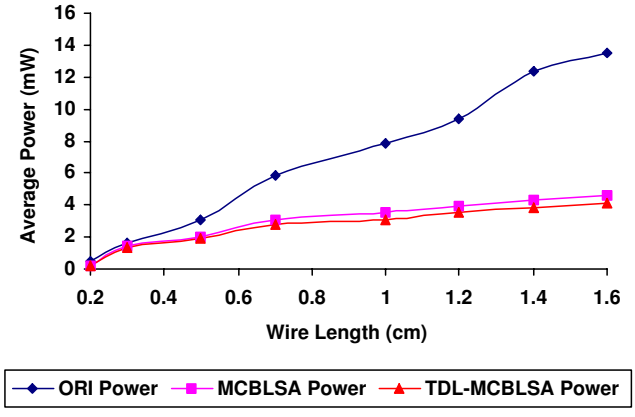

Fig. 5. Power Comparison of ORI, MCBLSA and TDL-MASDLC Schemes

B. Crosstalk Simulations

In this part, six different scenarios have been simulated to extensively test the crosstalk characteristic of the TDL-MASDLC scheme. The aggressors in each of these cases have been made perfectly out-of-phase to simulate the worst-case situation. The cases have been described below followed by the results.

Case 1: The ORI and TDL-MASDLC interconnects, 1.2cm in length and pulsed by a 1GHz signal, are laid out separately with no coupling. This simulation gives the noise-free base values for delay in each of these schemes.

Case 2: A full-swing aggressor is placed as close as possible to one of the TDL wires on the same layer as shown in Fig. 6. This case analyzes the effect of lateral-coupling with a full-swing aggressor on the TDL-MASDLC scheme.

Case 3: In this case, the effect of cross-layer coupling, when

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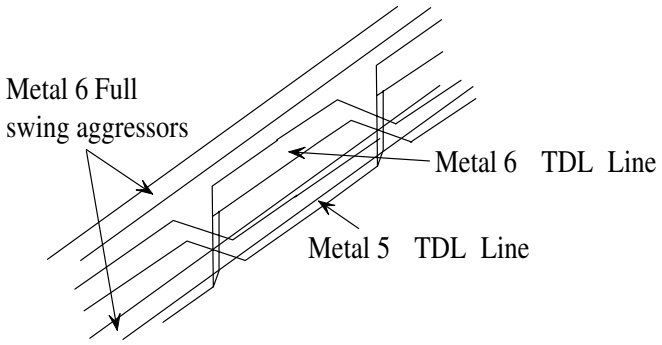

Fig. 6. Coupling between TDL and ORI wires as in Case 2

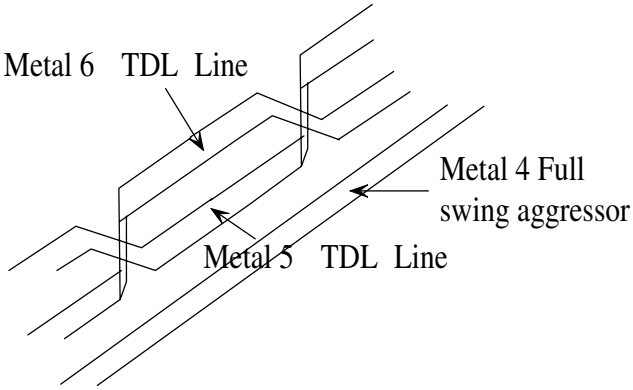

Fig. 7. Coupling between TDL and ORI wires as in Case 3

a full-swing aggressor is coupled to the TDL wires from a layer beneath is considered. As shown in Fig. 7, the TDL wires are laid on metals 5 and 6 while the ORI aggressor is placed beneath the TDL wires, in metal 4.

Case 4: Two full swing metal 6 aggressors, placed on either side of the metal 6 TDL wire are laid out to analyze the effect of multiple full swing aggressors on the TDL-MASDLC scheme.

Case 5: The setup in this case also has two full-swing aggressors, one placed above and the other below the TDL interconnects.

Case 6: The effect of coupling between low swing wires under the TDL-MASDLC scheme is analyzed in this case. Two pairs of TDL-MASDLC scheme interconnect wires are laid out close to each other to determine the effect of coupling between them.

The six cases were simulated and the effect of crosstalk on the receiver end waveform was measured in terms of the induced delay and pulse width. The simulation results are tabulated in Table II.

As seen from Table II, case 4 with same layer multiple full-swing aggressors represents the worse-case coupling situation, with a 23% delay variation. As expected, the signal distortion at the receiver end is seen to be the highest in this case. As seen from the results, the pulse width is reduced by 23%, compared to 68% in the full-swing scheme. The slew rate of the signal is not affected since the full-swing signal is regenerated afresh at the receiver end. Appropriate sizing of the output driver will ensure the desired slew rate. The input to the TDL-MASDLC

TABLE II
CROSSTALK SIMULATION RESULTS FOR THE TDL-MASDLC SCHEME

Case	Delay (ps)	Pulse Width (ns)
1	526.6	0.8958
2	612.1	0.8116
3	620.1	0.7839
4	650.6	0.6873
5	640.5	0.7242
6	636.2	0.7535

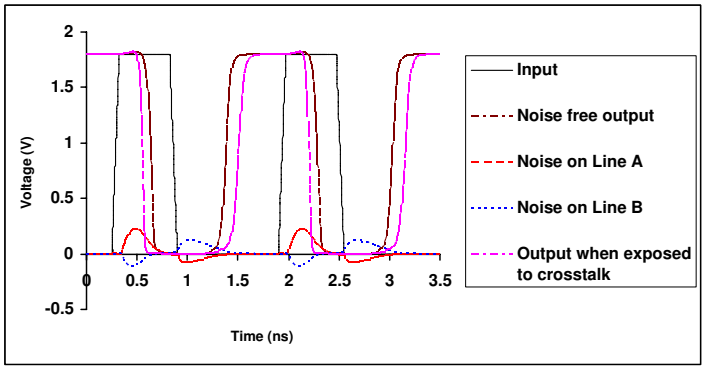

Fig. 8. Input, Noise and Receiver-end Waveforms for Case 4

interconnects, the noise waveform and the signal regenerated at the receiver end for the setup described in case 4 is shown in Fig. 8.

C. Reliability Analysis of the TDL-MASDLC scheme

Here, we present simulations to test the reliability of the TDL-MASDLC scheme. The effect of variation in process, temperature and supply voltage on the delay of the TDL-MASDLC interconnect is simulated. Fig. 9 shows the change in delay of the TDL-MASDLC scheme under different process variations. While TT indicates a normal process, SS, FF, SF and FS indicate various combinations of slow/fast P and slow/fast N.

The TDL-MASDLC scheme was simulated for various temperature and delay measured in each case. The temperature range simulated was -55degC to 125degC. The variation in

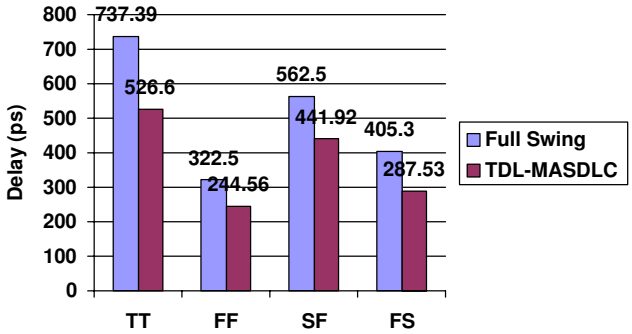

Fig. 9. Effect of Process Variation on TDL-MASDLC scheme

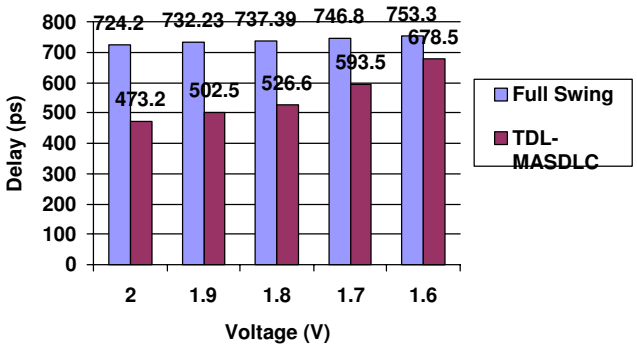

Fig. 10. Effect of Supply Voltage Variation on TDL-MASDLC Scheme

delay was seen to be less than 5%. Fig. 10 shows the change in delay with variation in supply voltage for the full swing and TDL-MASDLC schemes. From the figure, it is evident that while the full-swing scheme does not exhibit significant change in delay with variation in supply voltage, the TDL-MASDLC interconnect delay reduces with increase in supply voltage. However, the absolute delay in the TDL-MASDLC scheme is seen to be less than that in the full swing scheme.

V. Conclusion

We presented a new interconnection scheme for on-chip global interconnects and simulated it extensively for various cases. Simulation results indicate that the proposed TDL-MASDLC interconnection scheme has better delay and power characteristics compared to the prior schemes over a wide range of wire lengths. Simulations for noise immunity indicate that the delay variations in this scheme has reduced to 23% from 68% in the ORI scheme. Various cases of crosstalk have been simulated to test the robustness of the TDL-MASDLC scheme. Compared to the ORI scheme, the TDL-MASDLC scheme has 21% and 29% less delay in the nominal and worst cases. Our scheme was also simulated for change in delay with variation in process, temperature and supply voltage. The change in delay due to process variations in the TDL-MASDLC scheme is seen to follow the same variation in delay of the ORI scheme. The delay does not exhibit significant changes with variation in temperature.

The delay of TDL-MASDLC scheme decreases with increase in supply voltage. However, the absolute delay is always less than that of ORI scheme in the supply voltage range of 1.6-2.0V. The above results indicate that the TDL-MASDLC interconnection scheme is an appropriate choice for the VDSM interconnects. It is seen to lower power consumption, reduce delay and delay variation, and increase noise immunity compared to the conventional full swing scheme. It is robust under process, temperature and supply voltage variations which increases its reliability. Hence the TDL-MASDLC interconnection scheme is an appropriate choice for on-chip VDSM global interconnections.

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