CSCE 713: Advanced Computer Architecture
"Topics in High Performance Parallel Architectures"
Schedule Code: 589785
Meeting Times: Tuesday, Thursday 2:00 – 3:15
Location: Swearingen 2A22
Instructor: Dr. Jason D. Bakos

Topics

This course will explore recent topics in high performance computer architecture. Specifically, we will focus on new architectures for achieving task- and thread-level parallelism with single-chip architectures. Many such architectures rely on new on-chip communication techniques that have given way to new paradigms for general purpose and reconfigurable computing.

Since the advent of microprocessors, continuing advancements in chip fabrication technology have driven computer architects into new directions for increasing parallelism. For example, as die area, integration density, and on-chip interconnect capacity have increased, microprocessor architectures have gone from exploiting instruction-level parallelism (with multiple-issue out-of-order speculative execution) to exploiting thread-level parallelism (with concurrent multi-threading). Now, many computer architects have turned their attention to chip multiprocessors (CMP), where two or more discrete processor cores are integrated onto a single die. While Intel and AMD each have recently released a first generation version of a CMP, many challenges remain for developing advanced larger-scale CMP architectures.

One challenge is to develop new techniques to handle inter-core communication and cooperation. CMP opens the door for new opportunities not previously possible with multiprocessor systems where processor cores were isolated on independent chips. For example, CMP creates new opportunities for advanced on-chip networking techniques that allow for lower average communication latencies. However, CMP is also inflicted with new classes of resource constraints such as power and off-chip I/O. Another emerging issue involves the design of high-speed on-chip interconnection networks. As the wavelength of on-chip signals shrink relative to the corresponding wire length, new problems have arisen concerning signal integrity and signal delay. New interconnect and network technologies are currently being developed to address these problems.

Finally, the same motivations that have driven chip multiprocessors and system-on-chip design have also increased interest in large-scale single-chip reconfigurable and adaptive architectures. These architectures face similar opportunities and challenges as CMP.

Course Organization

This course will be organized as a seminar course. During each class period, one or two students will present a relevant conference or journal paper. After the presentation, there will be a discussion and review of the paper. In addition, each student will be expected to develop a course project by the end of the term. This project may be a group effort and may consist of further investigation of any of the topics discussed in class.