

**CSCE 611**  
**Lab 3**  
**ALU: FPGA Verification**  
**Due Date: 10/4 (during class)**

**Design Requirements**

Your goal for this lab is to implement your ALU on the Cyclone 2 FPGA on the DE2 board and demonstrate its functionality through JTAG, as described in Tutorial 14.

**Project Submission**

Each group must demonstrate--using the JTAG script provided--the operation of their ALU on the FPGA board to the instructor during class on the due date.