

**CSCE 611**  
**Lab 2**  
**ALU: Post Place and Route Simulation**  
**Due Date: 9/29**

**Design Requirements**

Your goal for this lab is perform post-synthesis simulation of your ALU to determine the logic latency for each of the data paths shown in Table 1.

To measure the logic delay of a particular data path, you can use the following technique:

1. force the inputs and allow the output to stabilize,
2. change the input value (beginning of the data path) in such a way that guarantees that the output (end of the data path) will change, and
3. measure the time from the input transition to the corresponding final output transition.

You can measure the time difference in Modelsim by adding a second cursor by clicking the green circle in the lower-left corner of the wave window. This allows you to use one cursor to mark the change in input and the second cursor to mark the change in output. The time difference is shown at the bottom of the window.

<b>Data path</b>	<b>Operation</b>	<b>Latency (ns)</b>
A → R	ADD	
A → zero	ADD	
A → overflow	ADD	
A → R	SUB	
A → zero	SUB	
A → overflow	SUB	
A → R	ADDU	
A → zero	ADDU	
A → R	SUBU	
A → zero	SUBU	
A → R	SLT	
A → R	SLTU	
A → R	SLL	
SHAMT → R	SLL	
A → R	SRL	
SHAMT → R	SRL	
A → R	SRA	
SHAMT → R	SRA	
A → R	AND	
A → R	OR	
A → R	XOR	
A → R	NOR	

Table 1

**Project Submission**

Each group must submit:

1. A completed Table 1
2. Screenshots depicting the measurements for the three ADD operations (insert these images in the report document)

Submit your projects through the course Moodle site (<http://dropbox.cse.sc.edu>)