CSCE 611
Lab 1
ALU and Test Bench Design
Due Date: 9/20

Introduction

As discussed in class, designing a good test bench is an important component in behavioral design. In this lab you will design a test bench for your ALU.

Design Requirements

Your test bench must generate inputs to your ALU (**A**, **B**, **SHAMT**, **ALUOP**) and verify that the actual outputs (**R**, **ZERO**, **OVERFLOW**) are consistent with the expected results based on the input values.

Specifically, for each operation you must use an ASSERT statement to verify the value of **R**. For the arithmetic operations (ADD, SUB, ADDU, SUBU), you must also use an ASSERT statement to verify the values of **ZERO** and **OVERFLOW**.

Test Coverage

You must test all test cases outlined in Table 1. Note that many of the entries in the table are empty, left for you to figure out.

ALU Operation	Test Case	Inputs	Expected Outputs
Bitwise AND	Non-zero output	A=X"0F0F0F0F" B=X"FFFFFFFF" SHAMT=don't care	R=X"0F0F0F0F"
	All zero output	A=X"0F0F0F0F" B=X"F0F0F0F0" SHAMT=don't care	R=X"00000000"
	All one output	A=X"FFFFFFFF" B=X"FFFFFFFF" SHAMT=don't care	
Bitwise OR	All one output	A=X"0F0F0F0F" B=X"F0F0F0F0" SHAMT=don't care	
	Non-zero output	A=X"0F0F0F0F" B=X"00000000" SHAMT=don't care	
	All zero output		
Bitwise XOR	Invert bits of A by setting B to all ones, non-zero output		
	All one output		
	All zero output		
Bitwise NOR	Invert bits of A by setting B to all zeros, non-zero output		

	All one output		
	All zero output		
Shift left logical	Shift by non-zero number of bits		
	Shift by zero bits		
Shift right logical	Shift by non-zero number of bits		
	Shift by zero bits		
Shift right arithmetic	Shift positive value by non-zero number of bits		
	Shift negative value by non-zero number of bits		
Set on less than	A < B	A, B positive	R = X“00000001”
	A = B	A, B positive	R = X“00000000”
	A > B	A, B positive	
	A < B	A, B negative	
	A > B	A, B negative	
	A < B	A negative, B positive	
	A > B	A positive, B negative	
Set on less than unsigned	A = B		
	A < B	A(31) = 0, B(31) = 0	
	A < B	A(31) = 0, B(31) = 1	
	A > B	A(31) = 0, B(31) = 0	
	A > B	A(31) = 1, B(31) = 0	
Add	$0 < A + B \leq 2^{31}-1$ A > 0 B > 0		Overflow = ‘0’ Zero = ‘0’ R = A + B
	A + B = 0		
	$-2^{31} \leq A + B < 0$		
	$A + B < -2^{31}$		
	$A + B > 2^{31}-1$		
Add unsigned	$0 \leq A + B \leq 2^{32}-1$		
	A + B = 0		
Subtract	$0 < A - B \leq 2^{31}-1$ A > 0 B > 0		
	A - B = 0		
	$-2^{31} \leq A - B < 0$		
	$A - B < -2^{31}$		
	$A - B > 2^{31}-1$		
Subtract unsigned	$0 \leq A - B \leq 2^{32}-1$		

	A - B = 0		

Project Submission

Each group must submit:

1. The generated VHDL for their tester design.
   This file should be a single text file with an extension of .vhd
2. A completed table showing the chosen test bench values.
   This file should be a Microsoft Word or PDF file.

Submit your projects through the course Moodle site (http://dropbox.cse.sc.edu)