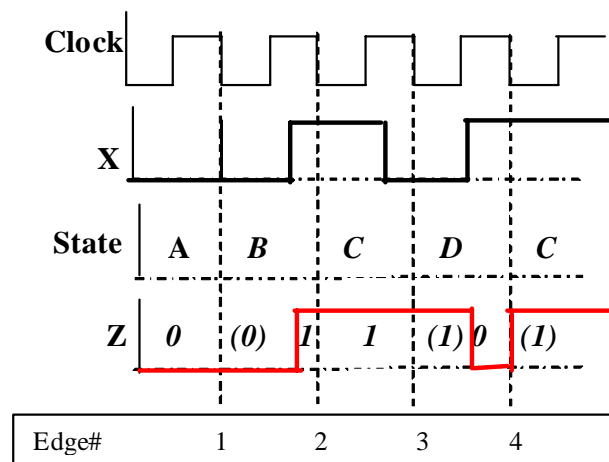


Quiz 10 CSCE 211 2009-04-22

1. The Mealy sequential device described by the following state table is in state *A* initially as shown below. Complete the state and output portions of the timing diagram in the figure below. For output *Z*, show both the waveform and the output sequence, including false outputs in parenthesis, as on p. 366 of the textbook. Assume that state transitions occur on the *negative (falling)* edge of the clock. Remember that input *X* and output *Z* are *present* values.

Present State	Next State/Present Output <i>S⁺/Z</i>	
	<i>X</i> = 0	<i>X</i> = 1
<i>S</i>	<i>B</i> /0	<i>A</i> /0
<i>A</i>	<i>B</i> /0	<i>A</i> /0
<i>B</i>	<i>B</i> /0	<i>C</i> /1
<i>C</i>	<i>D</i> /1	<i>A</i> /1
<i>D</i>	<i>B</i> /1	<i>C</i> /0



Answer:

See red waveform and values in italics in the picture above.

The indicated outputs are the ones immediately preceding the active (falling) clock edge. The outputs in parenthesis are the “false outputs” as described on p.366 of the textbook. In order, they are: 0 because present state is *A* and *X* = 0 immediately preceding the first falling clock edge; 1, because present state is *B* and *X* = 1 immediately preceding the second falling clock edge; 1, because present state is *C* and *X* = 0 immediately preceding the third falling clock edge; 0, because present state is *D* and *X* = 1 immediately preceding the fourth falling clock edge. The output sequence, with the false outputs in parenthesis, is: 0 (0) 1 1 (1) 0 (1).