Note Title 4/23/2009

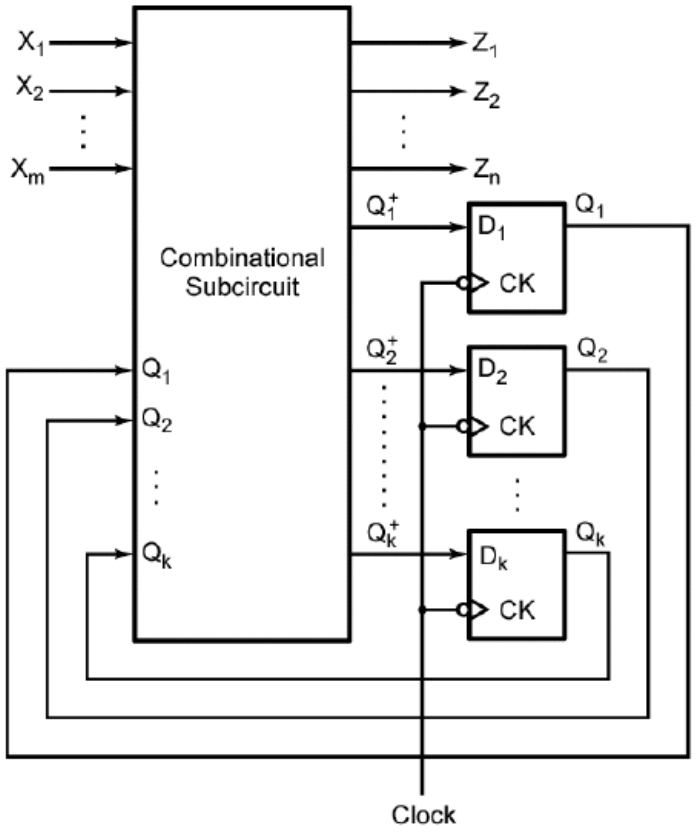


Figure 13-17:
General Model for Mealy Circuit Using Clocked D Flip-Flops

Outputs (Z_i, $i = 1..n$) are a function of states (Q_i, $i = 1..k$) and inputs (X_i, $i = 1..m$).

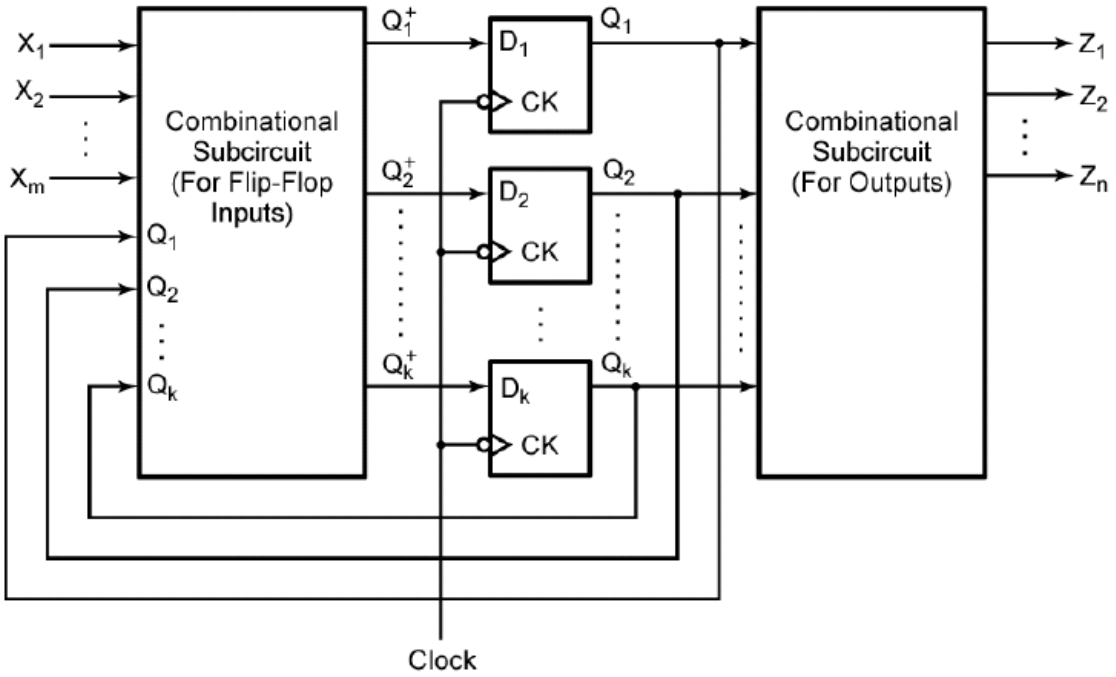
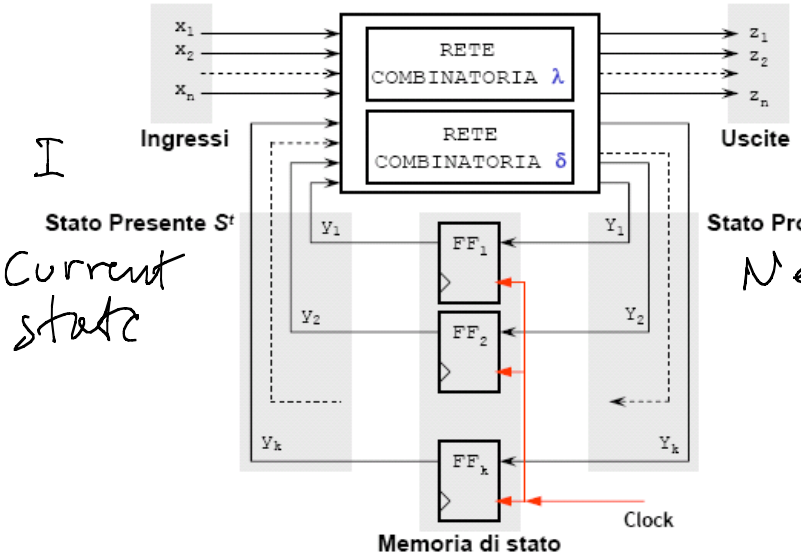


Figure 13-19: **General Model for Moore Circuit Using Clocked D Flip-Flops**

Outputs are a function of states only.

- Struttura generale di una macchina di Mealy:



I O

Current state

Next state

Memory

lambda

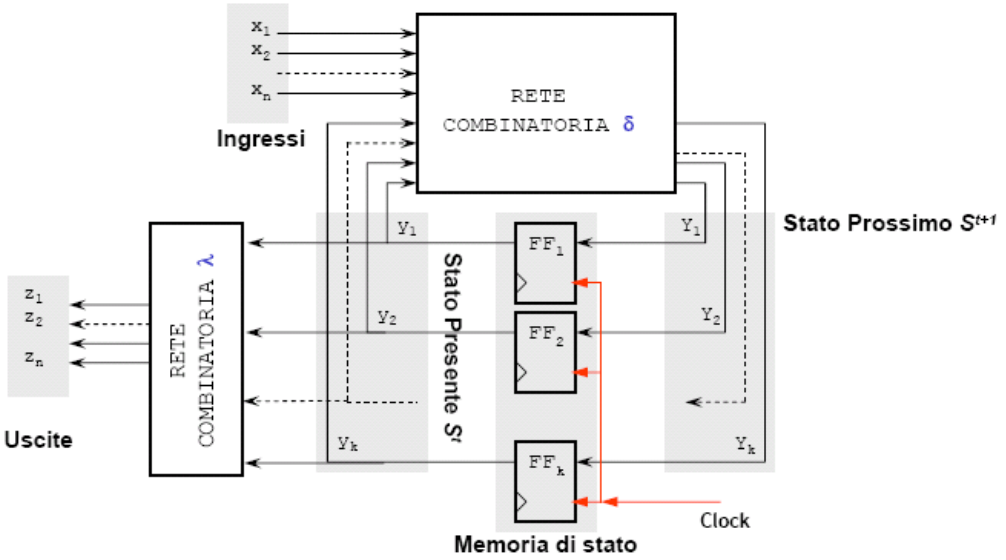
$z = \lambda(S, X)$

$S^+ = \delta(S, X)$

delta

(Text uses this notation at the end of Ch. 13)

- Struttura generale di una macchina di Moore:



$z = \lambda(S)$

$S^+ = \delta(S, X)$

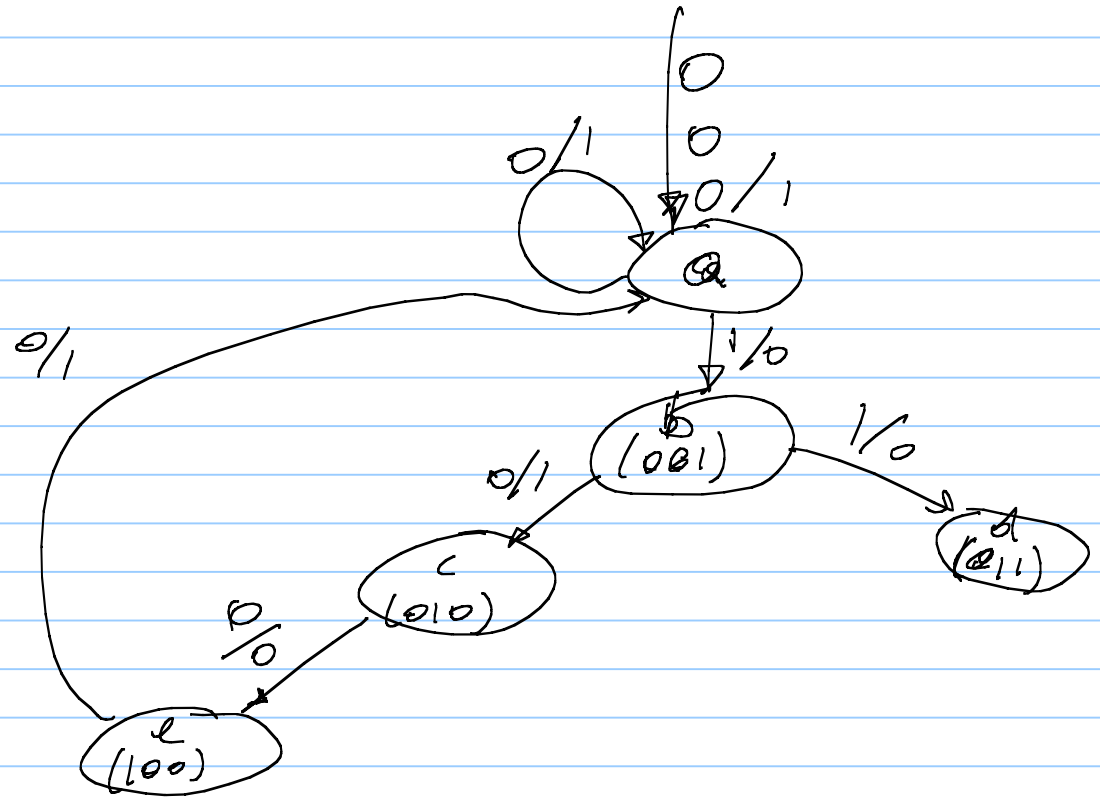
(text uses this notation at the end of Ch. 13)

Note: for both Mealy and Moore machines, the synthesis of δ depends on the type of flip-flop used; the synthesis of λ does not depend on the type of flip-flop used.

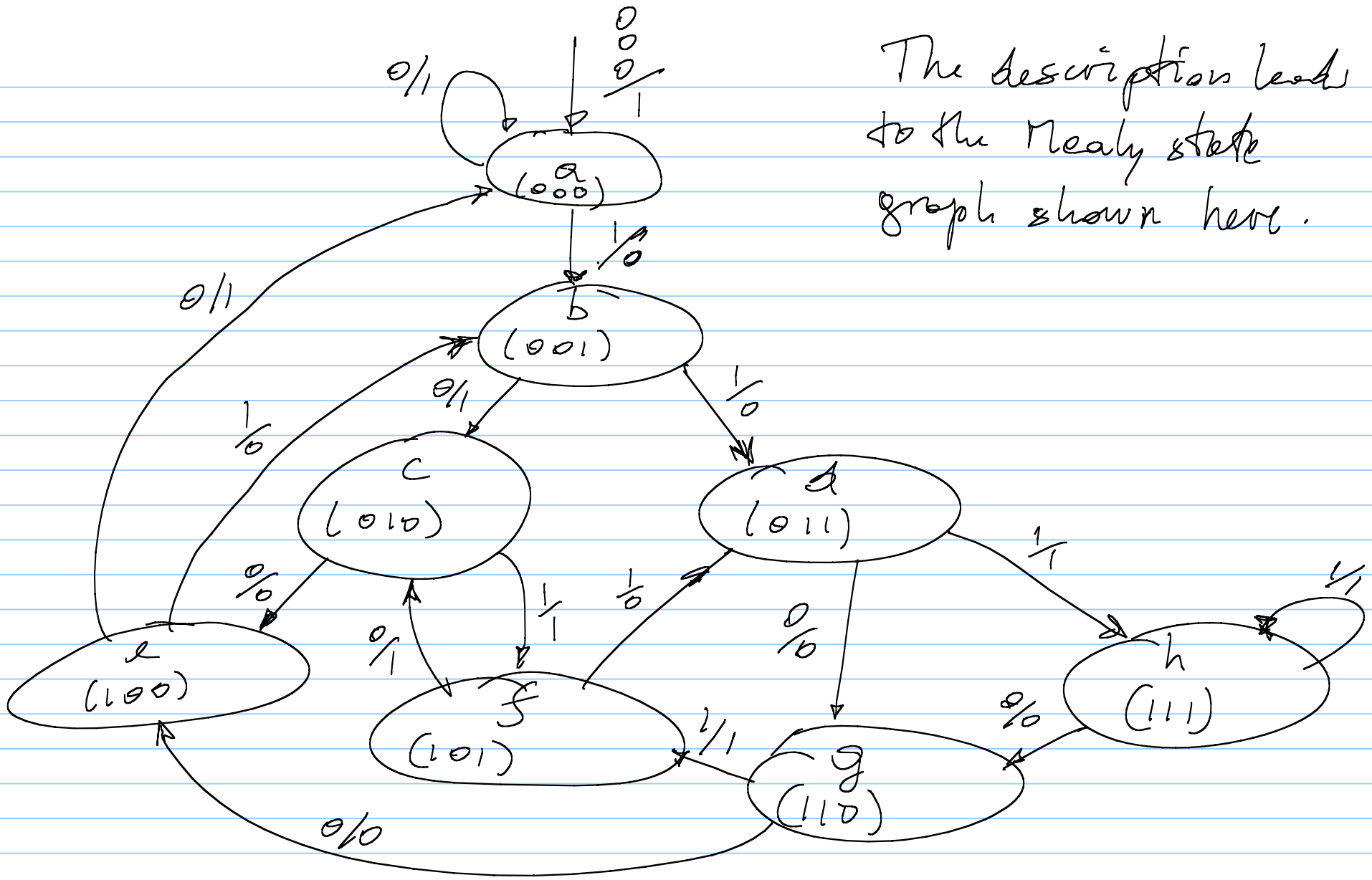
Example of design of a sequential circuit.
By "design" we mean synthesis, i.e., the process of converting the behavioral specification of a sequential machine to the (structural) specification of a sequential circuit.

The behavioral specification may be given in English, as a state graph, or as a table.
Our design problem is: Realize a sequential circuit with a single input (x) (in addition to the clock) and a single output (z). Output z at time t is 1 if and only if the value of x at the same time is equal to the value of x two instants before, i.e., $x(t) = x(t-2)$.

(a) Let us construct a Mealy state graph for the design problem above.



The description leads to the Mealy state graph shown here.



(b) From the state graph, we can construct (easily) the following state and output table

S \ X	0	1
a	a, 1	b, 0
b	c, 1	d, 0
c	e, 0	f, 1
d	g, 0	h, 1
e	a, 1	b, 0
f	c, 1	d, 0
g	e, 0	f, 1
h	g, 0	h, 1

(S^+, Z)

This table has duplicate rows, namely (a, e), (b, f), (c, g), (d, h). Therefore, one could reduce the state and output table to:

S \ X	0	1
a	a, 1	b, 0
b	c, 1	d, 0
c	a, 0	b, 1
d	c, 0	d, 1

(S^+, Z)

Only 4 states are required.

One can also show that 4 states are required.

However, we will not minimize the number of states for this example.

(c) Since we have 8 states (a, ..., h), we need 3 flip-flops.
(In general, you need $\lceil \log_2 m \rceil$ flip-flops for m states.)

ceiling of $\log_2 n$

We assign flip-flops arbitrarily for this example. Let the flip-flop states be $Y_1\ Y_2\ Y_3$. The assignment is:

	Y_1	Y_2	Y_3
a	0	0	0
b	0	0	1
c	0	1	1
d	0	1	0
e	1	0	0
f	1	0	1
g	1	1	1
h	1	1	0

The state transition table becomes

$Y_1Y_2Y_3$ \ x	0	1
000	000, 1	001, 0
001	011, 1	010, 0
011	100, 0	101, 1
010	111, 0	110, 1
100	000, 1	001, 0
101	011, 1	010, 0
111	100, 0	101, 1
110	111, 0	110, 1

(d) We choose D flip-flops and write the transition table for each flip-flop.

y_2y_3 \ xy_1	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$Y_1^+ = y_2$

y_2y_3 \ xy_1	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

$Y_2^+ = y_2y_3 + y_2y_3'$

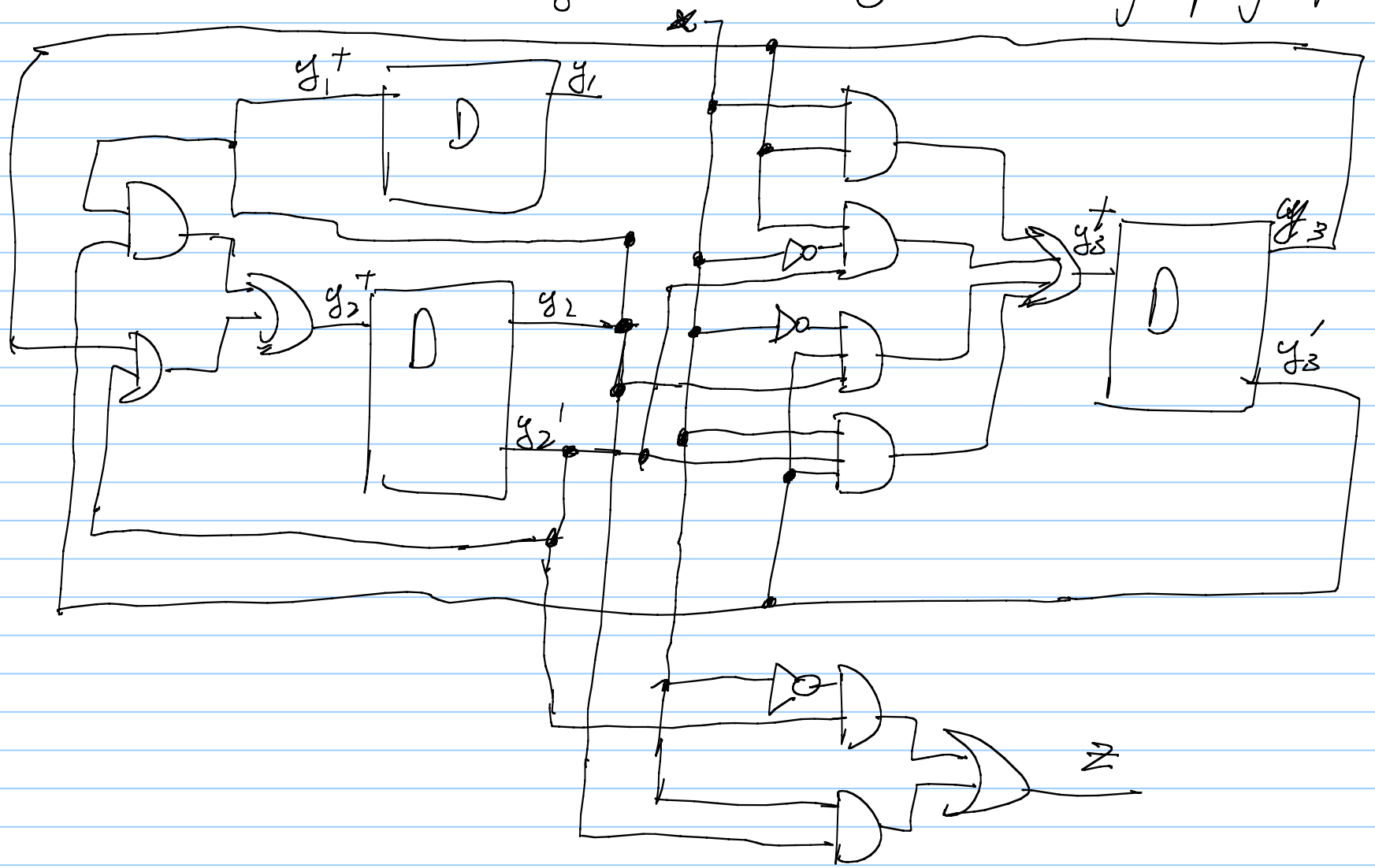
y_2y_3 \ xy_1	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	0	0	1	1
10	1	1	0	0

$Y_3^+ = x'y_2'y_3 + x'y_2y_3' + xy_2'y_3' + xy_2y_3$

y_2y_3 \ xy_1	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	0	0	1	1
10	0	0	1	1

$Z = x'y_2 + xy_2$

e) Realize the circuit using available gates and flip-flops



If flip-flop other than D-flip-flops are used, one needs an extra step from state transition table to flip-flop inputs, as shown in the example below, in which two S-R flip-flops are used.

Tabella delle transizioni

y_0y_1 \ I	0	1	U
00	01	11	00
01	10	11	01
11	01	10	10
10	10	00	11

Y_0Y_1 = stato prossimo
next state

Z

Tabella delle eccitazioni del FF SR

Q	Q*	C	S	R
0	0	0	–	–
1	1	0	–	–
0	0	1	0	–
0	1	1	1	0
1	0	1	0	1
1	1	1	–	0

Tabella delle eccitazioni con FF SR

y_0y_1 \ I	0	1	U
00	0-,10	10,10	00
01	10,01	10,-0	01
11	01,-0	-0,01	10
10	-0,0-	01,0-	11

S_0R_0 S_1R_1 Z
inputs to the SR flip-flops

⇒ Karnaugh maps may then be used to design the combinatorial circuits for
S_0 as a function of y_0, y_1, I
;
R_1 " " " " " " "
Z " " " " " " "

Equivalent states and minimization