Some hints for test 2 (take-home test)



HW

$D_0$ $D_0$

$D_1$ $D_1$

$D_2$ $D_2$

$D_3$ $D_3$

$S_1$ $S_0$

$S_1 S_0$

$D_4$ $D_0$

$D_5$ $D_1$

$D_6$ $D_2$

$D_7$ $D_3$

OEN

OEN

$S_1 S_0$

$Y$

$Y$

$Y$
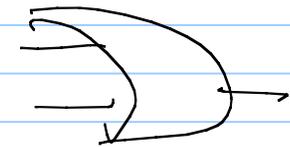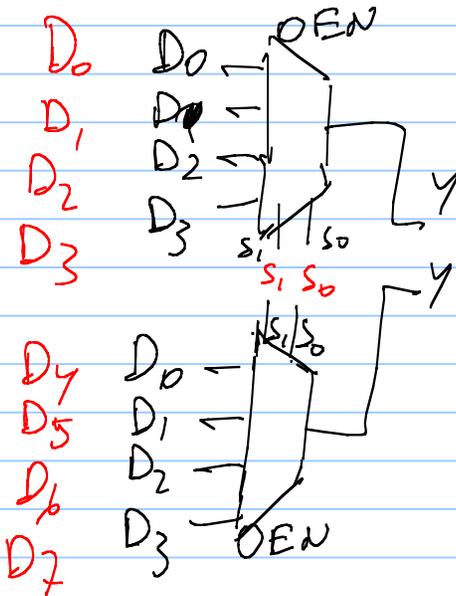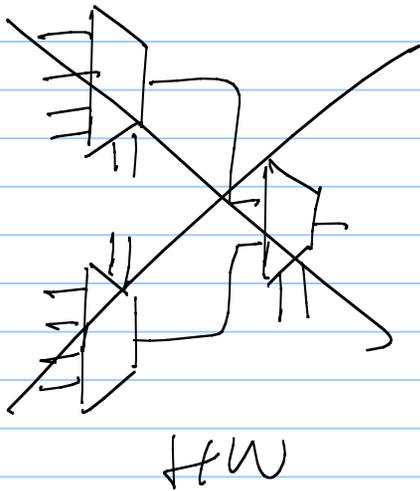
$S_2$

Circuit 3 will be posted before next class
It will be due Wednesday of next week.

**This chapter in the book includes:**

We already analyzed the Set Reset latch

$0 \rightarrow 1$

$1 \rightarrow 0$

$\Delta T1$

$\Delta T3$

$\Delta T2$

$0 \rightarrow 1$

S — SR Asincrono — Q'

R — — Q
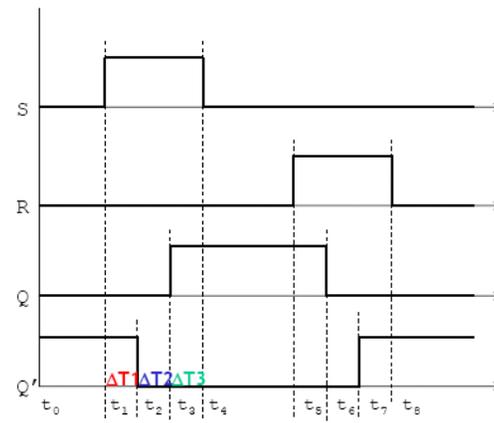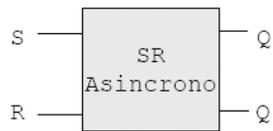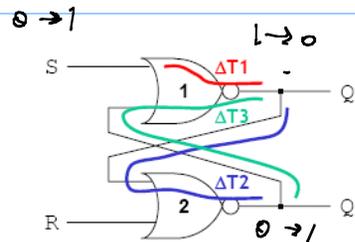
Delays in timing diagram

- 5 -

[Sanni]

Four different description of the behavior of the S-R latch

not in Ch. 11 of our textbook

Tabella delle transizioni

SR
Q   00  01  11  10
0   0   0   –   1
1   1   0   –   1

| S | R | Q* |
|---|---|----|
| 0 | 0 | Q  |
| 0 | 1 | 0  |
| 1 | 0 | 1  |
| 1 | 1 | –  |

Tabella delle eccitazioni

| Q | Q* | S | R |
|---|----|---|---|
| 0 | 0  | 0 | – |
| 0 | 1  | 1 | 0 |
| 1 | 0  | 0 | 1 |
| 1 | 1  | – | 0 |

Diagramma Temporale
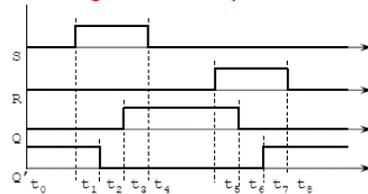
Espressione logica

$Q* = S + R'Q$
Con vincolo $S=R\neq1$

Q*: stato prossimo
Q : stato presente

[Sanni]          - 11 -
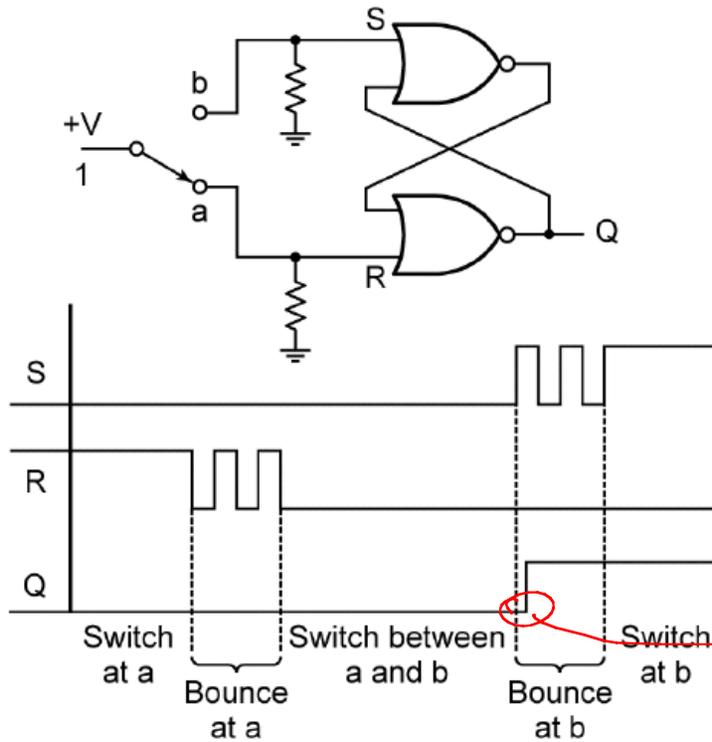
Figure 11-9: **Switch Debouncing with an S-R Latch**

After this short delay, the output of this debounced double-throw switch stays at 1, even though S bounces between 1 and 0.
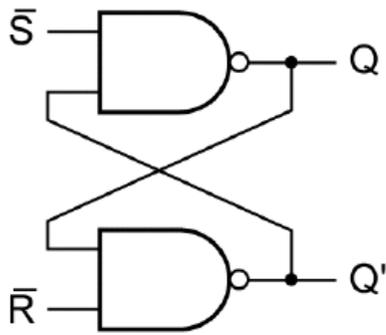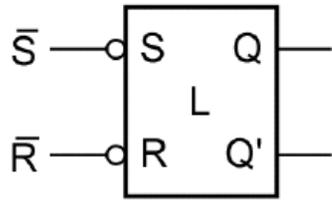
| $\bar{S}$ | $\bar{R}$ | $Q$ | $Q^+$ |
|---|---|---|---|
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | — } inputs not |
| 0 | 0 | 1 | — } allowed |

**Figure 11-10:** $\overline{\text{S}}$-$\overline{\text{R}}$ **Latch**

Dual of
S-R latch

# Gated D Latch



(a)

(b)
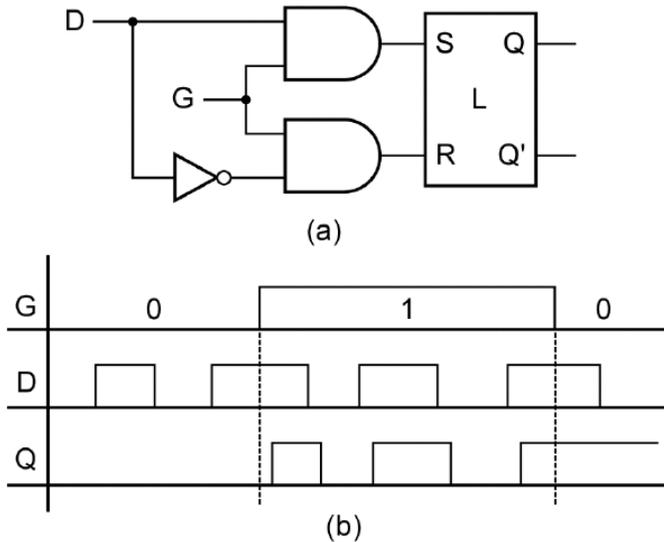
Figure 11-11: **Gated D Latch**



| G | D | Q | Q⁺ |
|---|---|---|----|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

The GDQ/Q+ table uses the header $GDQ \mid Q^+$.

Figure 11-12 (left): **Symbol and Truth Table for Gated Latch**



| Q \ GD | 00 | 01 | 11 | 10 |
|--------|----|----|----|----|
| 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 |

$$Q^+ = G'Q + GD$$

Figure 11-12 (continued)

→ Characteristic equation of the gated D latch. When $G = 1$, the input D is passed "transparently" to the Q output. When $G = 0$, there is no state change.

(a) Rising-edge trigger
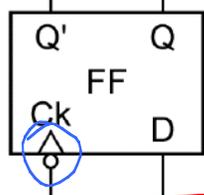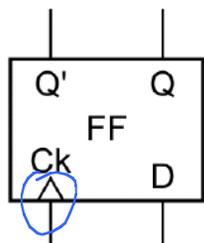
$0 \to 1$ transition

(b) Falling-edge trigger

$1 \to 0$ transition

| D Q | Q$^+$ |
|-----|-------|
| 0 0 | 0 |
| 0 1 | 0 |
| 1 0 | 1 |
| 1 1 | 1 |

(c) truth table

$$Q^+ = D$$

Figure 11-13: **D Flip-Flops**

In a flip-flop, the output only changes in response to the clock transitioning from 0 to 1 ("rising-edge trigger") or 1 to 0 ("falling edge trigger").
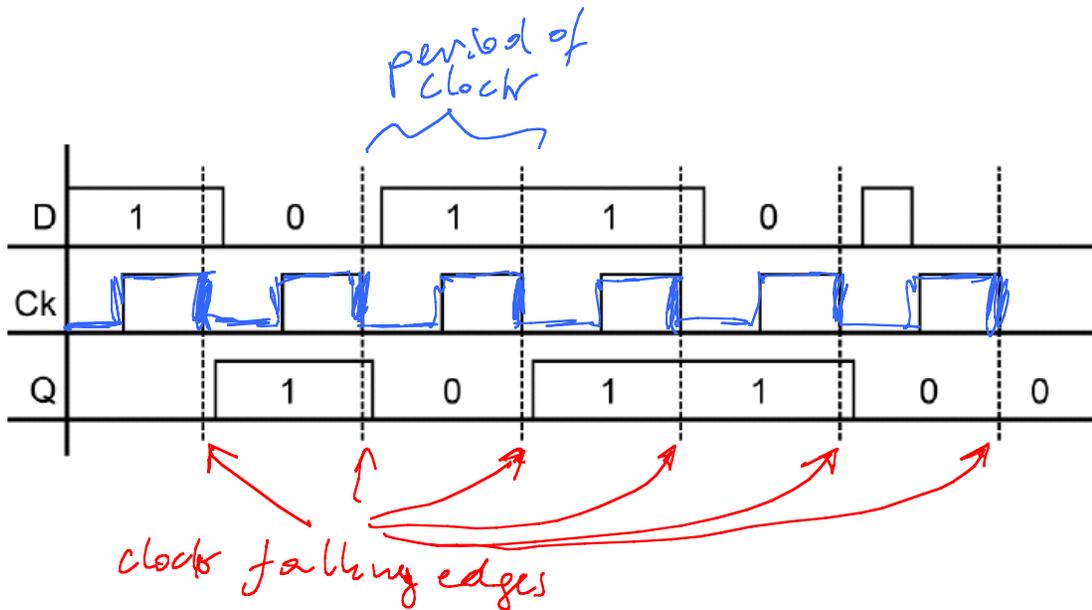
**Figure 11-14:** **Timing for D Flip-Flop (Falling Edge Trigger)**

period of Clock

clock falling edges

Timing is critical for flip-flops !
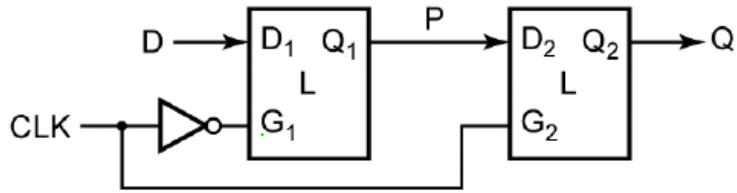
(a) Construction from two gated D latches



active edges

(b) Time analysis
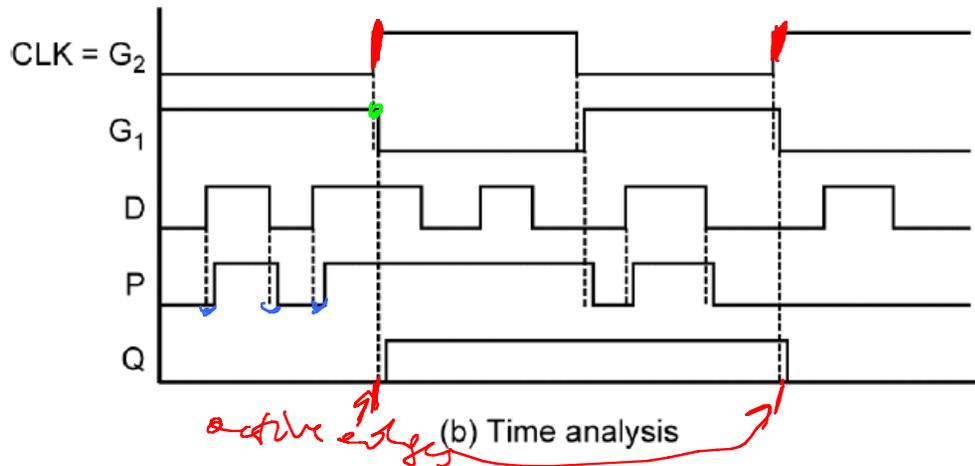
*Figure 11-15:* **D Flip-Flop (Rising Edge Trigger)**
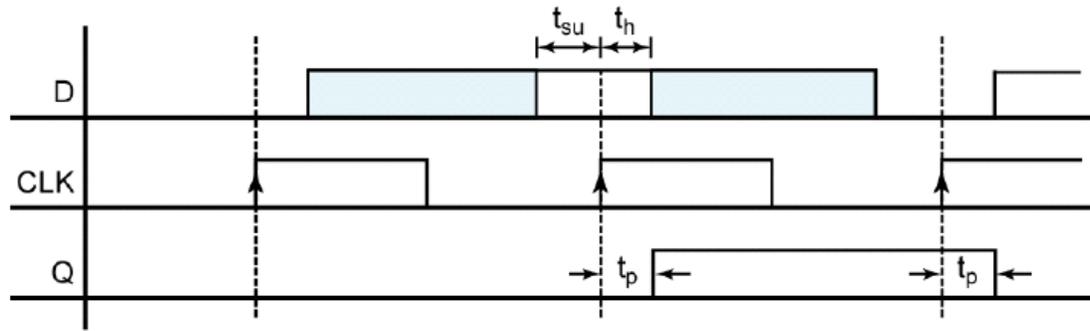
**Figure 11-16: Setup and Hold Times for an Edge-Triggered D Flip-Flop**

$t_{su}$ : set up time — time that D must be stable before the active edge of the clock

$t_h$ : hold time — time that D must be stable after the active edge of the clock

If setup and hold times are not respected, the flip-flop behavior is unpredictable.

$t_p$ is the propagation delay time, from the time the clock changes to the time the output Q changes.
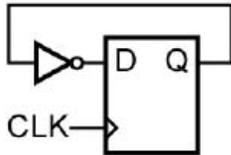
(a) Simple flip-flop circuit
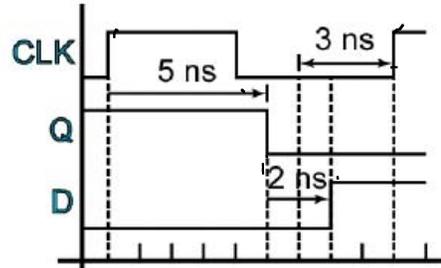


(b) Setup time not satisfied
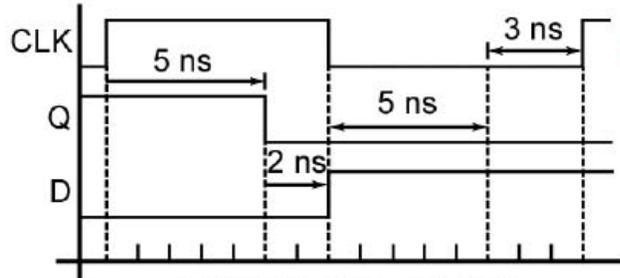


(c) Setup time satisfied
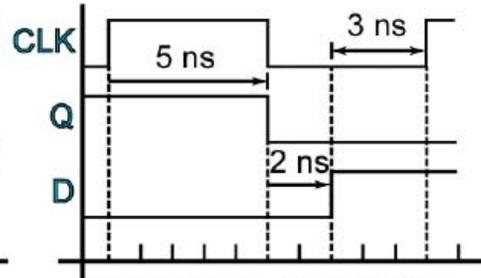


(d) Minimum clock period

*Figure 11-17:* **Determination of Minimum Clock Period**

5ns propagation delay for f-f
3ns setup time for f-f
2ns propagation delay for the inverter

(b) 9 ns (4+5)

(c) 15ns (7+8)

(d): 10ns (5+5)
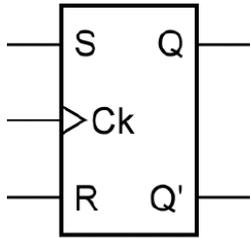
Operation summary:
   S = R = 0       no state change
   S = 1, R = 0    set Q to 1 (after active Ck edge)
   S = 0, R = 1    reset Q to 0 (after active Ck edge)
   S = R = 1       not allowed

*Figure 11-18:*  **S-R Flip-Flop**

$$Q^t = S + R'Q \quad (SR = 0)$$
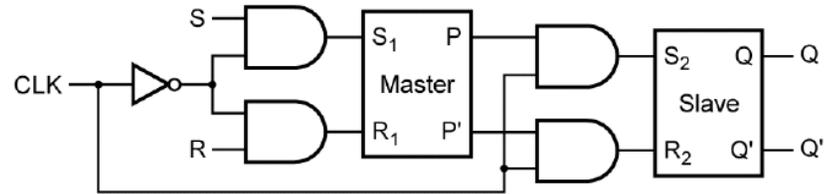


(a) Implementation with two latches
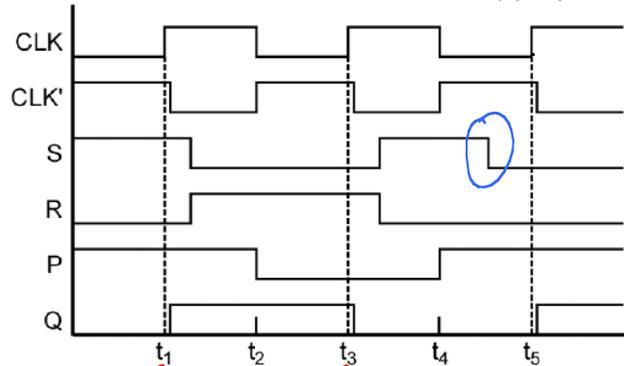
(b) Timing analysis

*Figure 11-19:*  **S-R Flip-Flop Implementation and Timing**

active clock edges
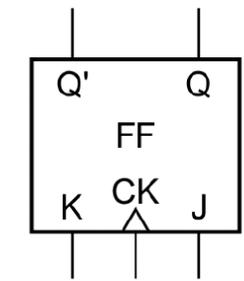
(a) J-K flip-flop

$$Q^+ = JQ' + K'Q$$

(b)

| JKQ | Q$^+$ |
|-----|-------|
| 000 | 0 |
| 001 | 1 |
| 010 | 0 |
| 011 | 0 |
| 100 | 1 |
| 101 | 1 |
| 110 | 1 |
| 111 | 0 |

S-R flip flop behavior

Figure 11-20ab:  J-K Flip-Flop
(Q Changes on the Rising Edge)

©2004 Brooks/Cole
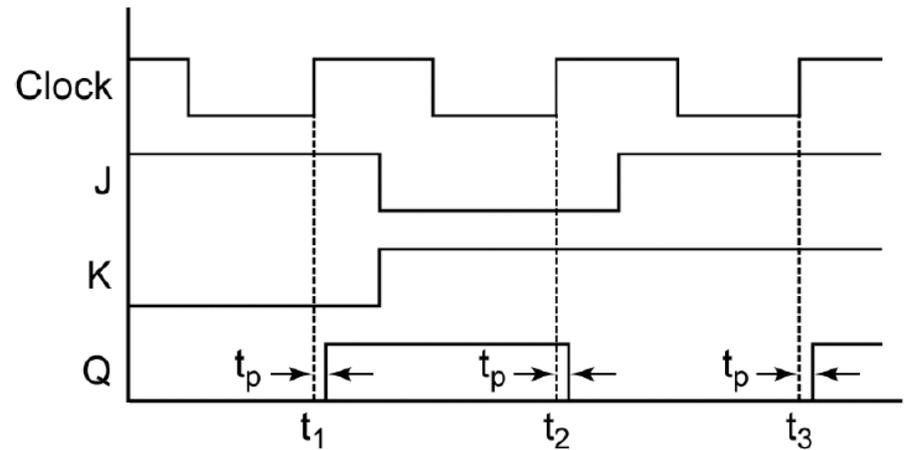
(c) J-K flip-flop timing

Figure 11-20c:  J-K Flip-Flop
(Q Changes on the Rising Edge)
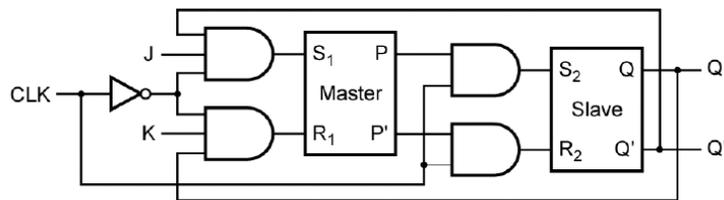
Figure 11-21:  Master-Slave J-K Flip-Flop
(Q Changes on Rising Edge)

| TQ | Q⁺ |
|----|-----|
| 0 0 | 0 |
| 0 1 | 1 |
| 1 0 | 1 |
| 1 1 | 0 |

(b)

(a)

$$Q^+ = T'Q + TQ' = Q \oplus T$$
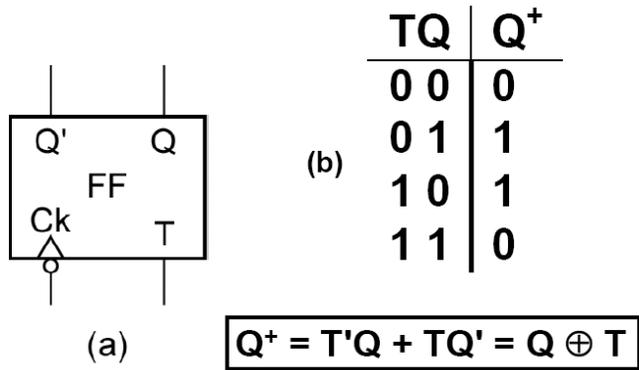
Figure 11-22ab: T Flip-Flop
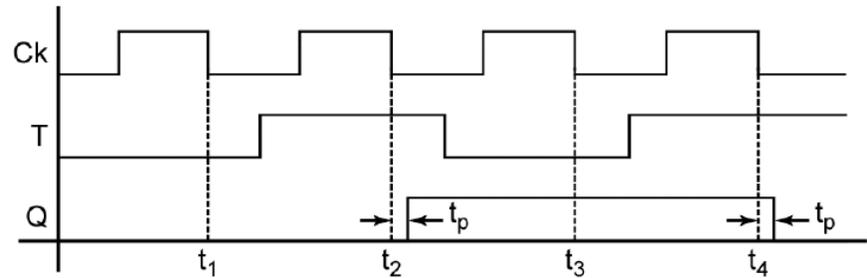


Figure 11-23: Timing Diagram for T Flip-Flop
(Falling-Edge Trigger)
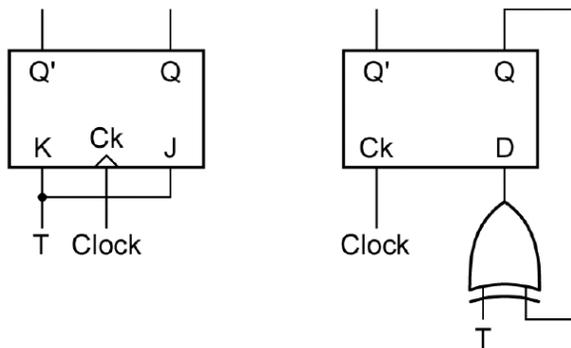
T for Toggle



(a) Conversion of J-K to T    (b) Conversion of D to T

Figure 11-24: Implementation of T Flip-Flops
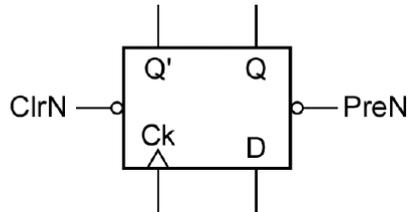
| CK | D | PreN | ClrN | Q$^+$ |
|----|---|------|------|-------|
| x | x | 0 | 0 | (not allowed) |
| x | x | 0 | 1 | 1 |
| x | x | 1 | 0 | 0 |
| ↑ | 0 | 1 | 1 | 0 |
| ↑ | 1 | 1 | 1 | 1 |
| 0,1,↓ | x | 1 | 1 | Q (no change) |

**Figure 11-25:** **D Flip-Flop with Clear and Preset**
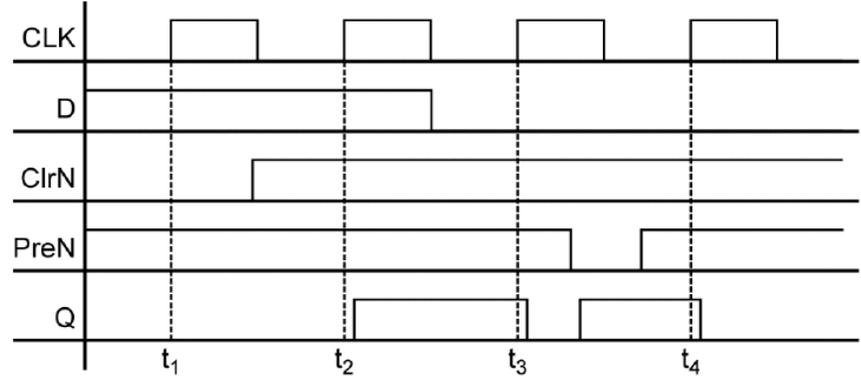


**Figure 11-26:** **Timing Diagram for D Flip-Flop with Asynchronous Clear and Preset**
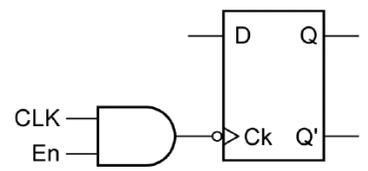


(a) Gating the clock
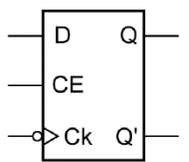
(b) D-CE symbol
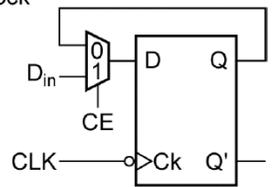
(c) Implementation

**Figure 11-27:** **D Flip-Flop with Clock Enable**