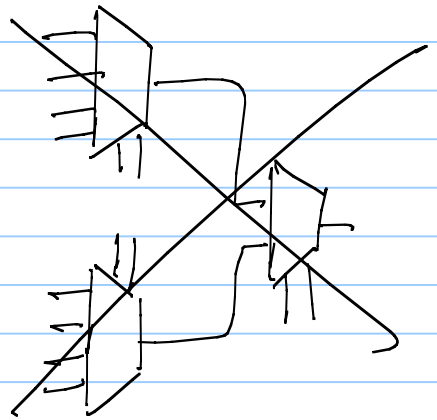
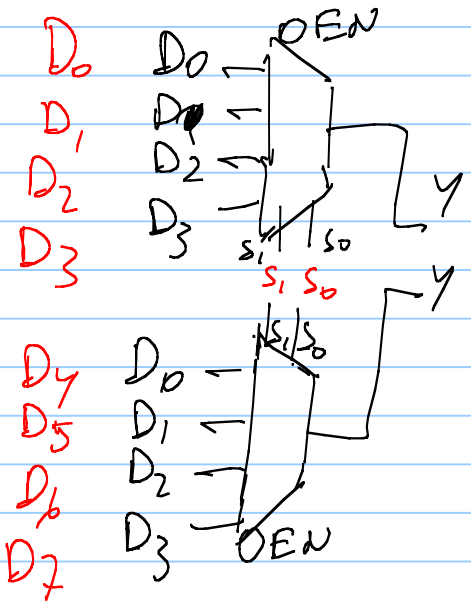
Note Title 4/15/2009

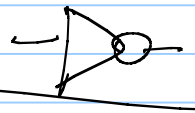
Some hints for test 2 (take-home test)



HW



y



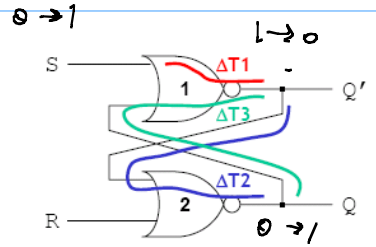
S_2

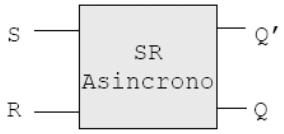
Circuit 3 will be posted before next class
It will be due Wednesday of next week.

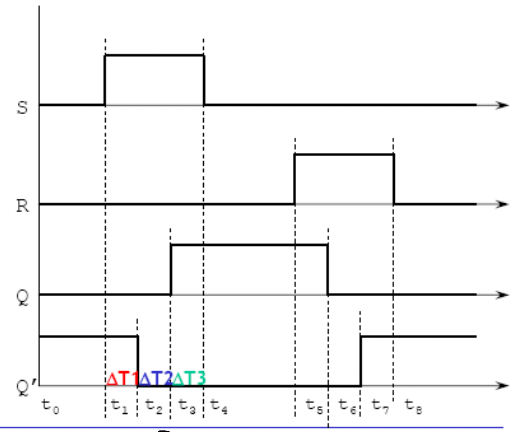
Note Title 4/14/2009

This chapter in the book includes:

We already analyzed the Set Reset Latch







Delays in timing diagram

- 5 -

[Sanni]

Four different description of the behavior of the S-R latch

Not in Ch. 11 of our textbook

Tabella delle transizioni

Q \ SR	00	01	11	10
0	0	0	–	1
1	1	0	–	1

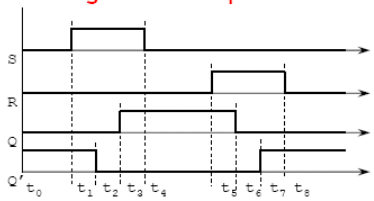
⟺

S	R	Q*
0	0	Q
0	1	0
1	0	1
1	1	–

Tabella delle eccitazioni

Q	Q*	S	R
0	0	0	–
0	1	1	0
1	0	0	1
1	1	–	0

Diagramma Temporale



Espressione logica

$Q^* = S + R'Q$

Con vincolo $S=R\neq 1$

Q*: stato prossimo
Q : stato presente

[Sanni]

- 11 -

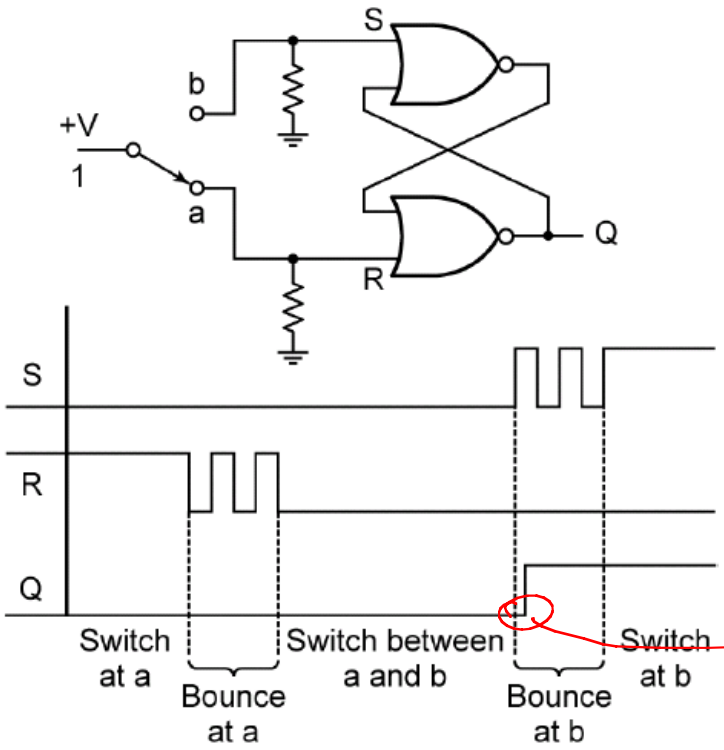
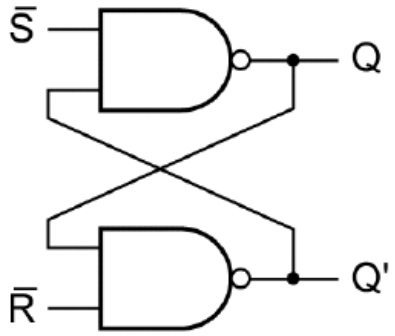
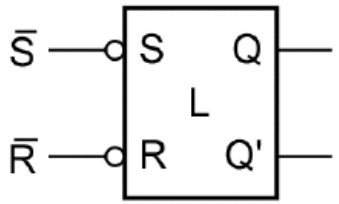


Figure 11-9: **Switch Debouncing with an S-R Latch**

After this short delay, the output of this debounced double-throw switch stays at 1, even though S bounces between 1 and 0.



(a)



(b)

$\bar{S}$	$\bar{R}$	Q	Q^+	
1	1	0	0	
1	1	1	1	
1	0	0	0	
1	0	1	0	
0	1	0	1	
0	1	1	1	
0	0	0	–	inputs not allowed
0	0	1	–	

Figure 11-10: **$\bar{S}$-$\bar{R}$ Latch**

Dual of S-R latch

Gated D Latch

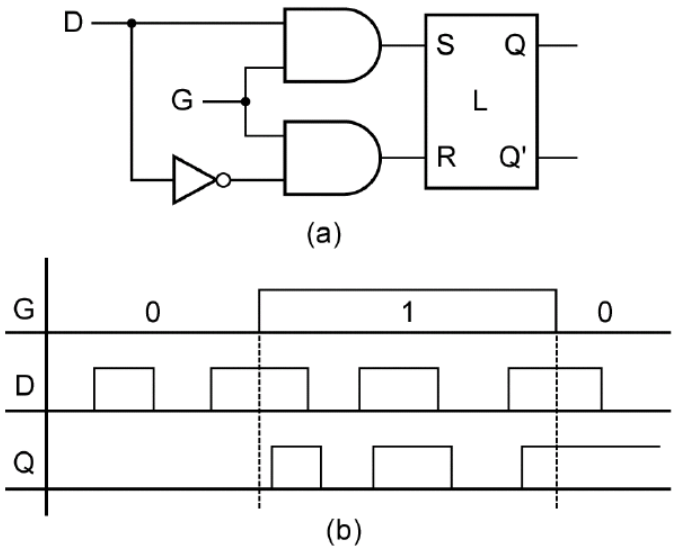
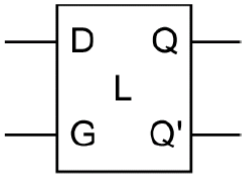


Figure 11-11: **Gated D Latch**



GDQ	Q^+
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	1
1 0 0	0
1 0 1	0
1 1 0	1
1 1 1	1

Figure 11-12 (left): **Symbol and Truth Table for Gated Latch**

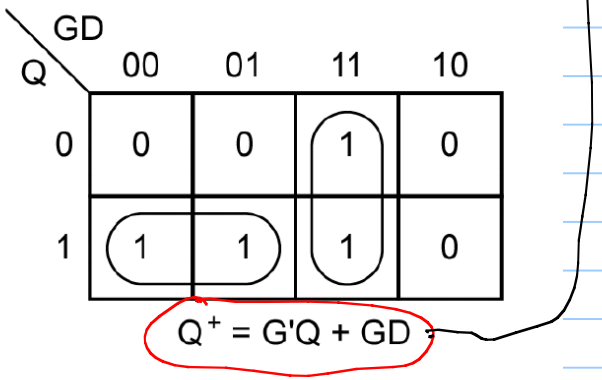
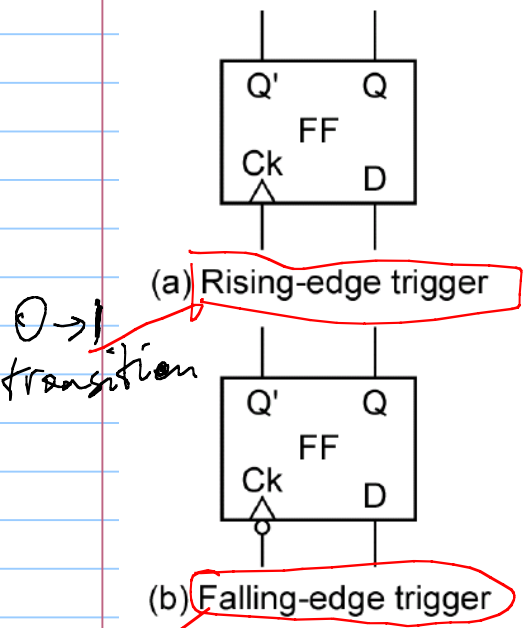


Figure 11-12 (continued)

→ Characteristic equation of the gated D latch. When G = 1, the input D is passed "transparently" to the Q output. When G = 0, there is no state change.



D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

(c) truth table

$Q^+ = D$

Figure 11-13: **D Flip-Flops**

In a flip-flop, the output only changes in response to the clock transitioning from 0 to 1 ("rising-edge trigger") or 1 to 0 ("falling edge trigger").

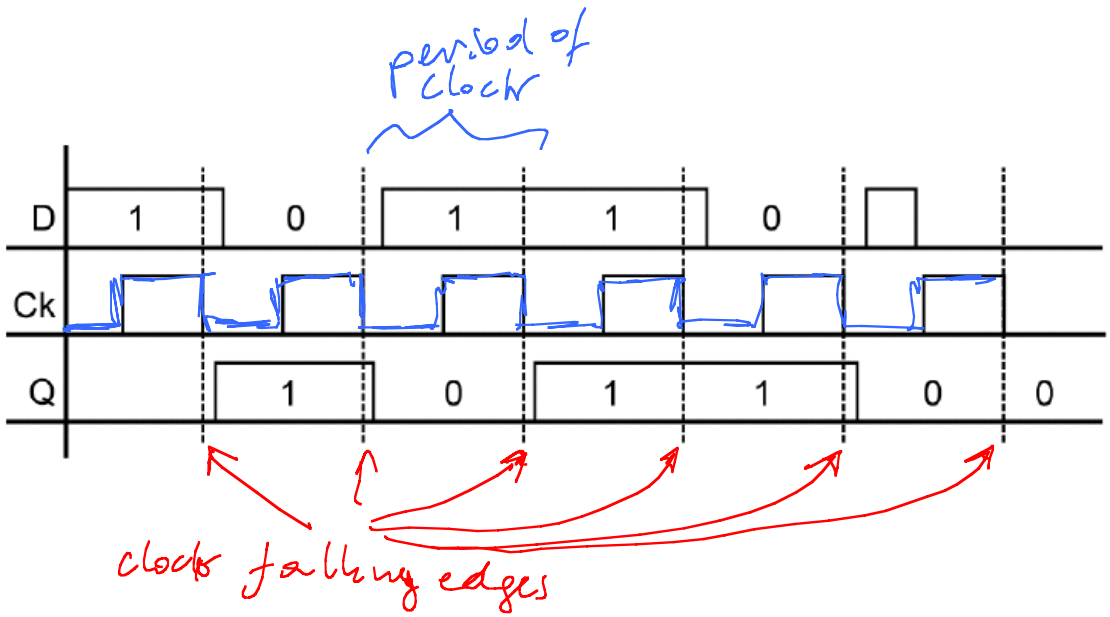
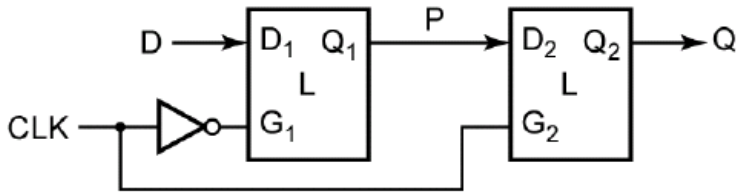
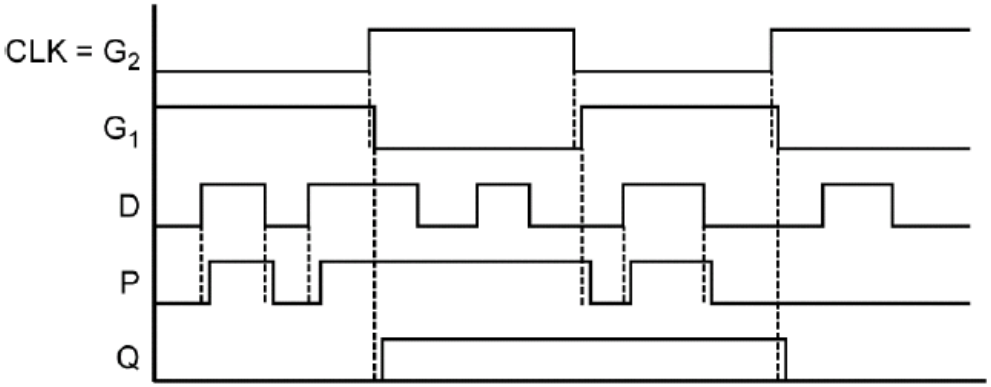


Figure 11-14: **Timing for D Flip-Flop (Falling Edge Trigger)**

Timing is critical for flip-flops!



(a) Construction from two gated D latches



(b) Time analysis

Figure 11-15: **D Flip-Flop (Rising Edge Trigger)**

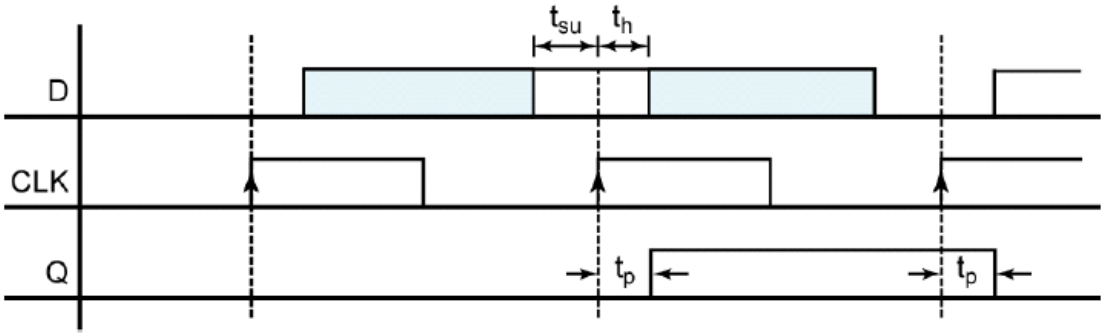


Figure 11-16: **Setup and Hold Times for an Edge-Triggered D Flip-Flop**

t_{su} : setup time — time that D must be stable before the active edge of the clock

t_h : hold time — time that D must be stable after the active edge of the clock

If setup and hold times are not respected, the flip-flop behavior is unpredictable.

t_p is the propagation delay time, from the time the clock changes to the time the output Q changes.

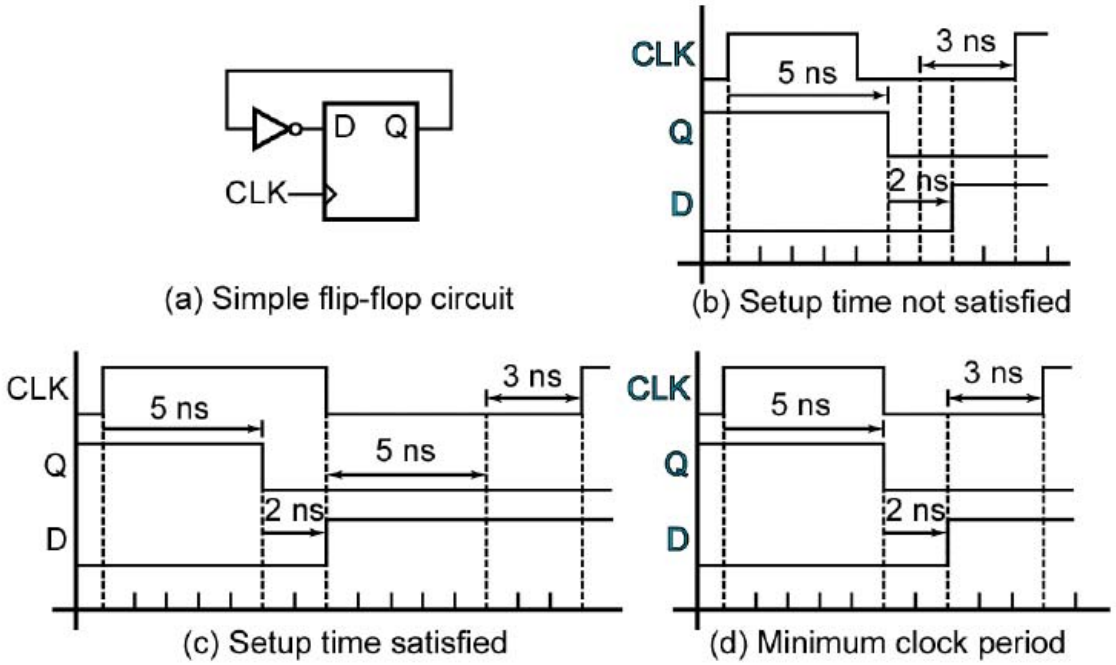
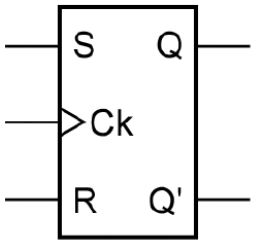


Figure 11-17: **Determination of Minimum Clock Period**

(b) 9 ns (4+5)

(c) 15ns (7+8)

(d): 10ns (5+5)



Operation summary:

S = R = 0	no state change
S = 1, R = 0	set Q to 1 (after active Ck edge)
S = 0, R = 1	reset Q to 0 (after active Ck edge)
S = R = 1	not allowed

Figure 11-18: **S-R Flip-Flop**

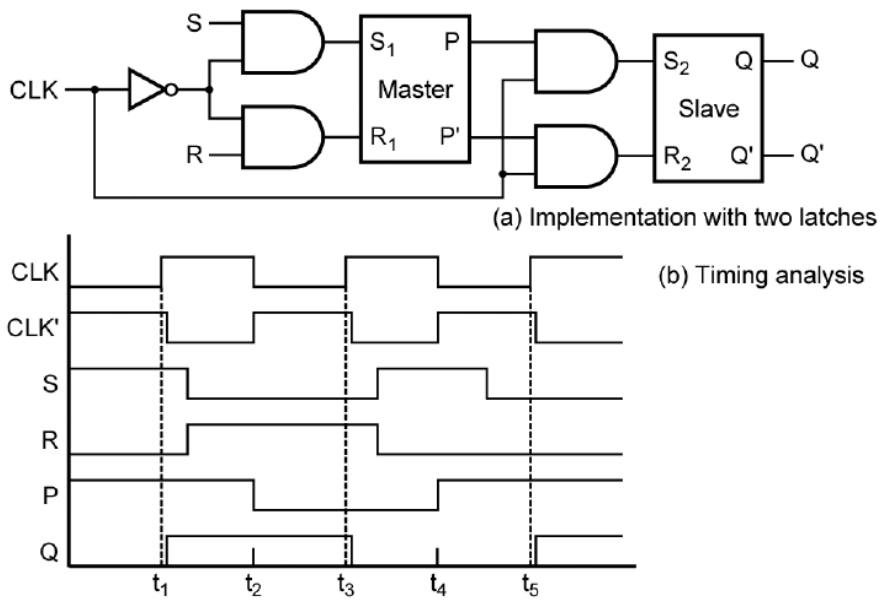
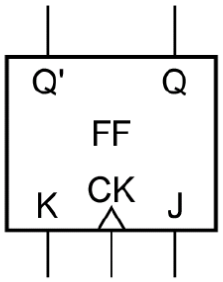


Figure 11-19: **S-R Flip-Flop Implementation and Timing**



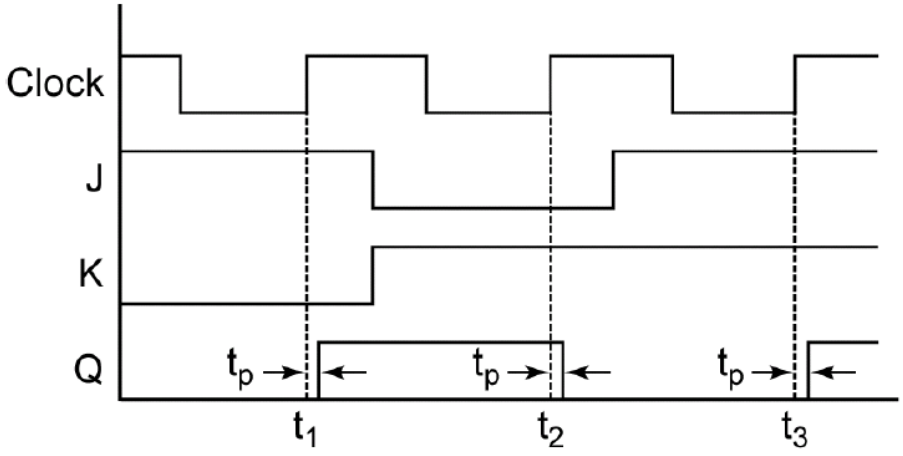
(a) J-K flip-flop

$$Q^+ = JQ' + K'Q$$

(b)

JKQ	Q^+
000	0
001	1
010	0
011	0
100	1
101	1
110	1
111	0

Figure 11-20ab: **J-K Flip-Flop**
(*Q* Changes on the Rising Edge)



(c) J-K flip-flop timing

Figure 11-20c: **J-K Flip-Flop**
(*Q* Changes on the Rising Edge)

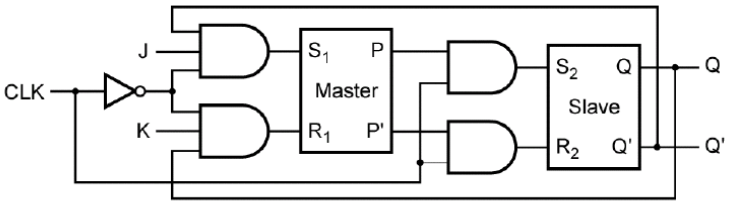
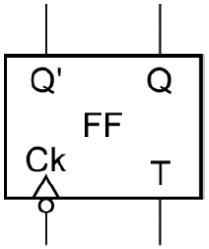


Figure 11-21: **Master-Slave J-K Flip-Flop**
(*Q* Changes on Rising Edge)



(a)

(b)

TQ	Q^+
0 0	0
0 1	1
1 0	1
1 1	0

$$Q^+ = T'Q + TQ' = Q \oplus T$$

Figure 11-22ab: **T Flip-Flop**

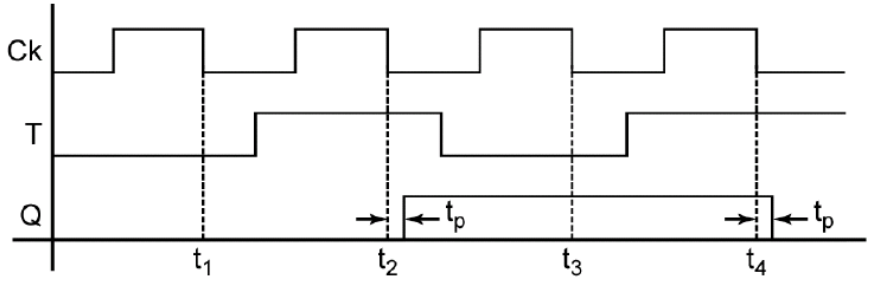
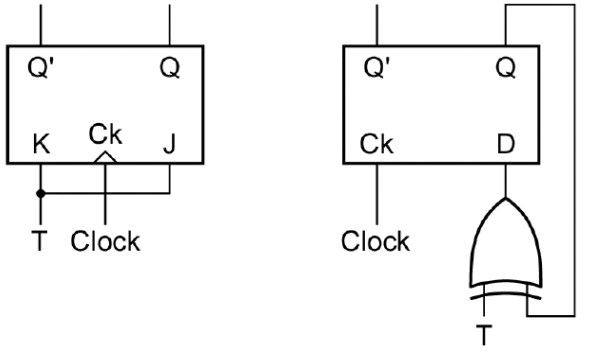
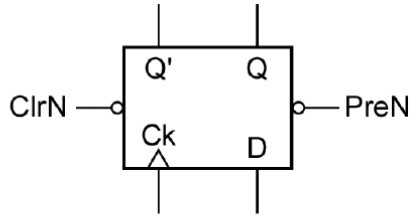


Figure 11-23: **Timing Diagram for T Flip-Flop (Falling-Edge Trigger)**



(a) Conversion of J-K to T (b) Conversion of D to T

Figure 11-24: **Implementation of T Flip-Flops**



CK	D	PreN	ClrN	Q^+
x	x	0	0	(not allowed)
x	x	0	1	1
x	x	1	0	0
↑	0	1	1	0
↑	1	1	1	1
0,1, ↓	x	1	1	Q (no change)

Figure 11-25: **D Flip-Flop with Clear and Preset**

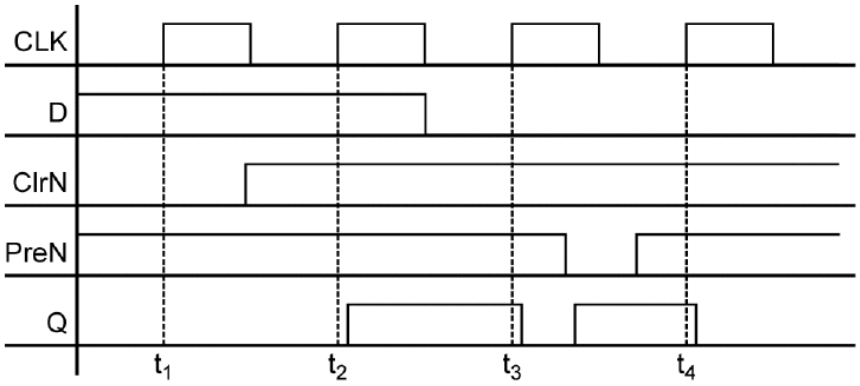


Figure 11-26: **Timing Diagram for D Flip-Flop with Asynchronous Clear and Preset**

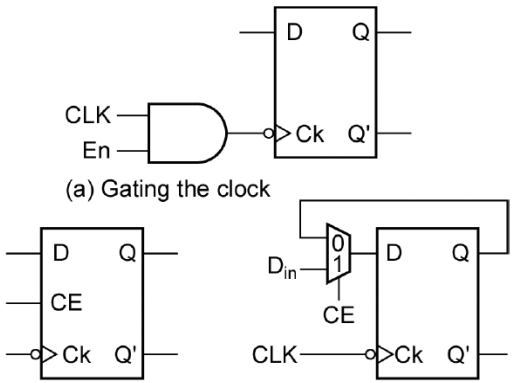


Figure 11-27: **D Flip-Flop with Clock Enable**